The LinCMOS™ Design Manual

1985

LinCMOS™ Applications and Data: Op-Amps, Comparators and Timers

TEXAS INSTRUMENTS

The LinCMOS™ Design Manual

By David P. E. Dale
Senior Applications Engineer
European Linear Product Dept. Bedford

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1. Introduction

Low power circuits, with their reduced operating temperature and enhanced reliability, allow smaller equipment sizes and have an impact on the total cost of system ownership. Low power operation also makes possible an increase in the number of applications for remote and battery or solar powered equipment. With the introduction of Texas Instruments' LinCMOS™ process the same system advantages that have been brought to logic and microcomputers by CMOS are now available to linear devices.

LinCMOS is a process that gives to linear devices a superior performance over metal-gate CMOS by utilizing polysilicon gates and an optimised 'N well' structure. Texas Instruments' range of LinCMOS operational amplifiers allow a trade-off between supply current and speed by providing a choice of three bias settings. For quads and duals the bias selection is made by device type and for singles by a user programmable pin. There are also versions available that will operate with a supply voltage down to one volt.

LinCMOS operational amplifiers all feature low and stable offset voltages and low input bias currents. High bias mode gives wider bandwidth and faster slew rate than most standard bipolar devices at a comparable supply current. While medium bias gives a similar performance and low bias pushes power consumption into the micro-watt region. They are designed to allow single supply operation with common mode and output voltage ranges that extend down to the most negative supply rail.

This manual describes Texas Instruments' range of LinCMOS operational amplifiers, timers and comparators and shows how they are applied in analogue circuits and systems.

Acknowledgement is made to the many other people in Texas Instruments whose help and ideas have added to the content and accuracy of this book.

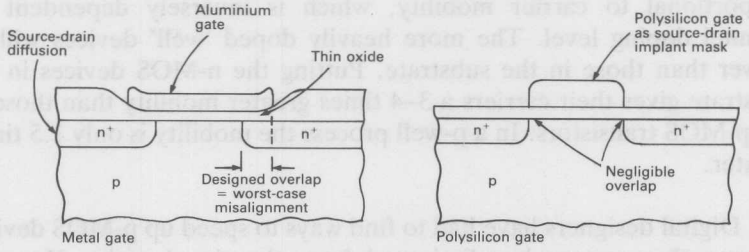
2. LinCMOS Overview

WHAT IS LinCMOS?

Texas Instruments' LinCMOS is a linear polysilicon-gate complementary-MOS process with p and n MOS transistors optimised to give bipolar type offsets and voltage swings. This process improves on the metal gate CMOS process in stability, speed and flexibility for linear building blocks such as operational amplifiers and comparators. The prime disadvantage of linear CMOS using the metal gate process has been the input transistors' threshold shift with time, temperature and applied gate voltage. This is caused by the migration of residual sodium ions in the gate oxide to the gate-oxide or silicon-oxide interface dependent on the polarity of the voltage stress. The resulting redistribution of charge causes threshold-voltage shifts that can be as great as hundreds of millivolts.

The LinCMOS process uses phosphorous doped polysilicon gates to counteract sodium drifts by trapping the sodium ions in the crystal structure. [Poly(crystalline)silicon is a layer of silicon with dislocations in the crystal structure. It is deposited by chemical vapour deposition in a similar manner to an epitaxial layer but at a lower temperature.] Op-amps may be built with voltage offset values of 2–5 mV with negligible drift and obtain these values without trimming.

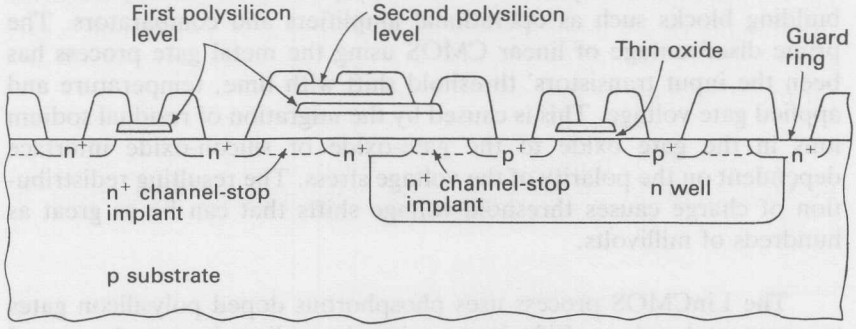
Fig. 2.1 Metal & Polysilicon gate alignment comparison.



Polysilicon gate CMOS devices also have a two or three times greater bandwidth than their metal gate counterparts because of a seven times reduction in gate capacitance. In a polysilicon gate process the

polysilicon is laid down first and provides a self aligned mask for the source/drain diffusion (see Figure 2.1). In the metal gate process the diffusions are formed first so the metal gate must overlap the drain and source regions to ensure channel coverage.

Fig. 2.2



LinCMOS. An n-well structure is used so that the n-MOS devices of this process sit in the substrate and run faster. Linear circuits also benefit from the stable offset voltages afforded by silicon gates. A second polysilicon layer adds wiring channels and capacitors.

The LinCMOS structure (Fig. 2.2) uses n-MOS devices in a p-type substrate and p-MOS devices in n-wells, unlike most CMOS digital circuits in which the structure is reversed. This optimises the inherently faster n-MOS devices at the expense of the p-types. Speed is proportional to carrier mobility, which is inversely dependent on channel doping level. The more heavily doped 'well' devices will be slower than those in the substrate. Putting the n-MOS devices in the substrate gives their carriers a 3–4 times greater mobility than those of the p-MOS transistors. In a p-well process the mobility is only 1.5 times greater.

Digital designers have had to find ways to speed up p-MOS devices because they cannot be eliminated from the signal paths. However bipolar analogue designers are accustomed to using faster vertical npn transistors in signal paths and living with slower lateral pnp devices. This strategy has been adopted for LinCMOS with n-MOS and p-MOS devices.

LinCMOS CIRCUIT DESCRIPTION

An operational amplifier's input circuit is its most critical section as from here the stability, offsets and noise are largely determined. As shown in Figure 2.3 the input stage comprises p-MOS inputs (P_1 and P_2) and a n-MOS current mirror (N_1 and N_2). These are large transistors made up of many small circular, cross coupled geometries which counteract process variations and take up about half the chip's area. The complex interconnection gives precise matching of the P_1P_2 and N_1N_2 pairs and minimises the effects of thermal and mechanical stresses on the stability of the input offset voltage. For critical applications where less than 2mV of offset is required null pins are provided on the singles for offset zeroing.

Large p-MOS transistors are used because noise voltage generated by MOS transistors is inversely proportional to area. Noise from the n-MOS pair is converted into noise current in the p-MOS drain circuit so the n-MOS transistors have very long channels to keep their transconductance ($g_m \propto W/L$) small. The ratio of g_{mp} to g_{mn} is maximised within the constraints of geometric and electrical trade offs to generate as little noise as possible.

Use of a p-MOS differential input pair allows the common mode range to include the most negative supply rail, 0 V, in single rail applications. This is made possible by the body effect, the modulation of the gate source voltage from the bulk side of the transistor (see Figure 2.1), which increases the p-MOS transistors threshold voltage. This keeps the p-MOS input pair and n-MOS mirror in current saturation when the gates are at 0V.

Transistor P_3 is the constant current source for the pair P_1P_2 and P_4 acts as a constant current load for the voltage amplifier N_3. Approximately half the voltage gain comes from the differential input stage comprising P_1P_2 with N_1N_2 as a current mirror active load. The other half comes from the N_3N_4 combination, N_3 for the positive output swing and N_4 for the negative output swing.

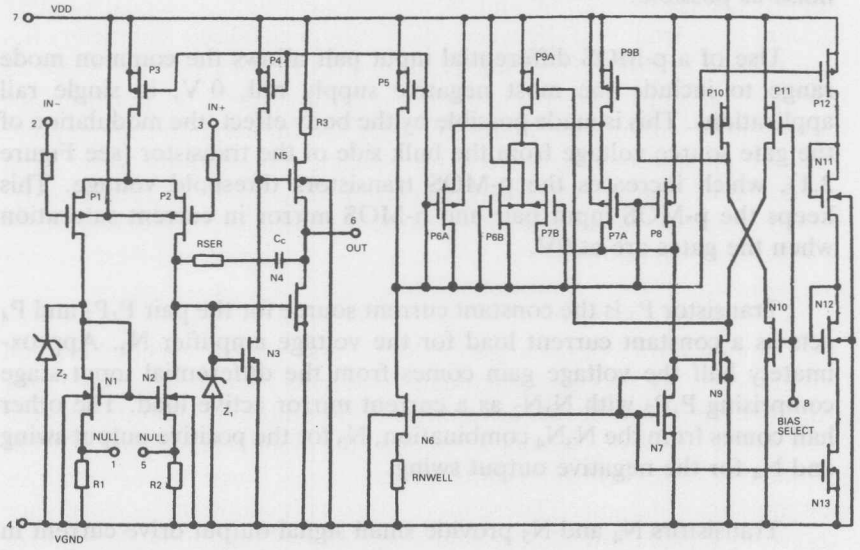
Transistors N_4 and N_5 provide small signal output drive current in class A. N_5 is connected as a source follower with drain resistor R_3 and the large N_4 as a bias current source. Transistor N_4 sinks large signal output currents. Zener diode Z_1 clamps N_4's gate to about 6V to limit the output current and give protection from shorts to V_{DD}. Zener diode

Z_2 matches Z_1's leakage currents and prevents the input stage shifting in response to temperature. Large output source current is provided by N_5 and limited by R_3 to give short circuit protection.

The internal frequency compensation capacitor C_c of 12pF is connected from the gate of N_3 to the drain of N_4 and controls the circuits high frequency roll-off to ensure stability in voltage follower configurations (see op-amps compared and stability sections).

The chip's supply current setting circuit allows quiescent current adjustment over three decades, 10 to 1000μA. Switching between currents is performed by transistor switches P_{9A} and P_{9B}. Connecting pin 8 to ground opens both P_{9A} and P_{9B} resulting in the high supply current mode. Connecting pin 8 to V_{DD} closes both P_{9A} and P_{9B} for low supply current operation. When pin 8 is connected to a voltage at least 0.8V above ground or below V_{DD} P_{9A} is closed and P_{9B} is open resulting in the medium current mode of operation.

Fig. 2.3 TLC271 schematic diagram.



Switches P_{9A} and P_{9B} select the current mode in the following manner: P_{9A} switches P_{6A} and P_{7A} into or out of the p-MOS mirror formed by P_5 and P_8, thus changing the width to length ratio of P_5 and P_8 with respect to P_3 and P_4. Since the P_5 diode is operating at a constant current, this alters the gate to source voltage of P_3 and P_4, to change the current by a factor of ten. Similarly, P_{9B} switches P_{6B} and P_{7B} into or out of the p-MOS mirror to change the current by an additional decade.

OPERATIONAL AMPLIFIERS COMPARED

Amongst the many characteristics of the idealised op-amp the requirement for infinite gain, input impedance and bandwidth are conceptually the most important. Some of the other characteristics, which have an importance more dependent upon the op-amps application, are: common mode range, output voltage swing, noise, slew rate, offsets etc. This list is not exhaustive but certainly should include low supply voltage operation and power consumption. Practical op-amp design is a trade off between the various idealised characteristics constrained by process technology, design restrictions and cost. General purpose op-amps have been optimised to give the best performance compromise within these limits. By using special design techniques and process enhancements devices for specific applications have been produced which trade-off other characteristics (usually including cost). When choosing an op-amp for a particular design the device selected will depend on which set of characteristics will give the best overall performance in the application.

Bipolar, BIFET, metal-gate CMOS, and CMOS versions merged with bipolar, are process technologies that have been used for op-amps. All have their own design advantages and limitations. Polysilicon gate LinCMOS op-amps, having overcome the major metal-gate CMOS problem of offset drifts and shifts, present a new range of 'best' features for the circuit designer. These more effectively allow the performance choice to include low voltage and single supply operation, low power consumption and speed (slew rate/bandwidth).

Table 2.1 gives a comparison between bipolar, BIFET and LinCMOS operational amplifiers.

Table 2.1

TECHNOLOGY	BIPOLAR[1]	BIFET[2]	LinCMOS (bias levels)		
			LOW	MEDIUM	HIGH
V_{CC} MAX REC	±15	±15	16	16	16
V_{CC} MIN REC	±5	±5	1	1	1
V_{CC} SPECFD	±15	±15	10**	10**	10**
V_{IO} mV	1–10	3–20	2–10	2–10	2–10
$\propto V_{IO}$ uV/degC	5–20*	10	0.7	2	5
I_{IO}	2–750nA	5p–2nA	1–300pA	1–300pA	1–300pA
I_{IB}	20–800nA	30p–10nA	1–600pA	1–600pA	1–600pA
V_{ICR} V	±13 or Vcc−1.5	±12	−0.2 to 9	−0.2 to 9	−0.2 to 9
V_{OM} IN 10kohms	24–26 or Vcc−1.5	24–77	0–7.8 RL=1M	0–7.8 RL=100k	0–7.8 RL=10k
A_{VD} V/mV	15–200	15–200	20–500	15–280	7.5–40
CMRR dB	70–90	70–76	70–88	70–88	65–82
I_{CC}	0.5–3.3mA	1.4–2.8mA	10–40µA	150–400µA	1–2.2mA
B_1 MHz	0.7–1	3	0.1	0.7	2.3
SR V/µS	0.5	13	0.04	0.6	4.5
en nV/Hz @ 1kHz	22*	18	70	38	30
in pA$\sqrt{Hz}$ @ 1kHz	0.55*	0.01	0.013*	0.013*	0.013*

Notes:

1. Bipolar figures are a composite over the range of types µA748 LM301, µA741, µA747, MC1458 & LM348 +/− supply rail and LM358, LM324 & MC3403 single rail.
2. Bifets are the TL080 series.
3. Commercial temp range characteristics are quoted.
4. Single figures are typicals, ranges are min (70 deg C) –typ (25 degC) or typ (25 deg C) – max (70 deg C) where appropriate.

*Not specified but typically.

**TLC25_ parts are available specified at 1V.

LinCMOS OP-AMP USER BENEFIT SUMMARY

Below are some brief notes that summarizes the user/application benefits of LinCMOS op-amps.

Single and Low Supply Voltage Operation

While giving good +/− supply rail performance, with a total supply voltage not exceeding 16V, the input and output are optimised for single supply operation. This is achieved with an input common mode range that includes GND ($-V_{DD}$ with +/− supplies) and an output range that pulls down to within a few millivolts of GND (with a load connected to GND). The TLC27_ range are specified to work with supply voltages down to 3V and thus will operate with the supplies that are commonly available for TTL and HCMOS. For maximum dynamic range single rail operation with 16V supplies should be used. For low power and battery operation the TLC25_ range are specified to operate with 1V total supply voltage.

Power consumption-Speed trade-off

High bias mode gives wider bandwidth (2.3MHz) and faster slew rate (4.5V/μs) than standard bipolar op-amps (especially single supply devices) for the same order of supply current. The enhanced bandwidth gives an increase in the open-loop to closed-loop gain ratio at a particular frequency improving accuracy, of for example filter circuits, or allowing higher frequency operation. Slew rate enhancement gives a wider large signal bandwidth and generally allows the implementation of faster circuits.

Medium bias mode gives standard bipolar op-amp performance at roughly a tenth of the supply current.

Low bias modes' prime advantage is the low power consumption with sufficient bandwidth and slew rate for basic sensor interface and audio applications.

Low bias currents

Low bias and offset currents allow: circuit simplification through the elimination of bias current balancing resistors, higher impedance circuits for greater accuracy (e.g. smaller higher tolerance capacitors) and circuit currents defined only by feedback components. Another

advantage is insignificant noise due to bias current (shot noise): noise is dominated by noise voltage and resistor noise.

Note:

For quad and dual op-amps the high, medium and low bias modes are respectively identified by 'no letter', 'M' or 'L' in the device number, e.g. TLC274 is high bias quad, TLC27M2 is a medium bias dual and TLC27L4 is a low bias quad.

Single op-amps (TLC271/251) are programmable by the level of voltage applied to the bias select pin 8. This voltage level has to be $-V_{DD}$ (or single supply GND) to give high bias mode, any voltage in the range $-V_{DD}$ +0.8V and $+V_{DD}$ −0.8V to give medium bias mode and $+V_{DD}$ to give low bias mode.

For further information see section 8 Data Sheets.

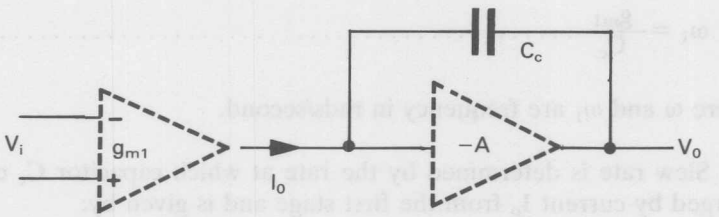
3. LinCMOS Design Characteristics Review

BASIC OP-AMP DESIGN CONSIDERATIONS

This section will give some insight into the basic gain, bandwidth and slew rate characteristics of LinCMOS op-amps in comparison with bipolar types.

A simple conceptual model (Figure 3.1) can be used to describe the internal circuit topology of the classical two stage op-amp. This is essentially an ac model and consists of a differential to single ended converter followed by an inverting amplifier with frequency compensating capacity C_c as shown in Figure 3.1.

Fig. 3.1 Classical two stage op-amp model.



At low frequencies, where the compensation capacity C_c has no effect, the op-amp's overall dc gain can be modelled by two cascaded gain stages. These stages for CMOS are voltage amplifiers with the gain of each stage given by $Av=g_m/g_o$ (g_m=transconductance, g_o=output conductance). For bipolar the first stage is transconductance and the second transresistance giving a voltage gain overall. Where the individual transistor loads reside determines the type of amplifier a stage forms (voltage, transconductance etc.). In CMOS circuits the input impedance of the following stage is so high that the load is only MOS transistor output conductance. In bipolar circuits the low input resistance of the following transistor stages dominate the loads. In general these can be designated R_{L1} and R_{L2} respectively wherever they appear to reside, and for this reason are not shown on Figure 3.1.

Op-amp d.c. voltage gain can be expressed to a first order as:

$$A_{d.c.} = (g_{m1}R_{L1})(g_{m2}R_{L2}) \quad \ldots\ldots (3.1)$$

To give the op-amp overall a.c. voltage gain the differential transconductance stage (Figure 3.1) drives current I_o into the 'virtual earth' node created by the inverting amplifier and the feedback compensating capacitor C_c. This capacitor, with it's associated Miller capacitance at this node, causes the amplifiers of the model to act for a.c. as transadmittance and transimpedance stages respectively. The voltage output is produced by current I_o flowing in C_c with the resulting op-amp a.c. voltage gain:

$$Av = \frac{V_o}{V_i} = \frac{g_{m1}}{I_o} \times \frac{I_o}{\omega C_c} = \frac{g_{m1}}{\omega C_c} \quad \ldots\ldots (3.2)$$

Equating this to 1 gives unity gain-bandwidth or gain-bandwidth product:

$$\omega_1 = \frac{g_{m1}}{C_c} \quad \ldots\ldots (3.3)$$

where ω and ω_1 are frequency in rads/second.

Slew rate is determined by the rate at which capacitor C_c can be charged by current I_o from the first stage and is given by:

$$\text{Slew rate SR} = \frac{dV_o}{dt} = \frac{I_o}{C_c} \quad \ldots\ldots (3.4)$$

substituting for C_c from (3.3)

$$SR = \frac{I_o\omega_1}{g_{m1}} \quad \ldots\ldots (3.5)$$

Circuit time constants for a particular process will determine the frequency compensation (C_c) required in order to keep the circuit stable with a satisfactory phase margin. This is usually specified at a gain of unity and sets the unity gain frequency, ω_1. Other parameters that control the limits on slew rate are from (3.5) g_{m1} and I_o and these have a fixed relationship dependent on process technology. For example in the bipolar process g_m is directly proportional to transistor emitter current

I_e (corresponding to I_o above) and is given by:

$$g_m = \frac{qI_e}{KT} = \frac{I_e}{26mV} \text{ (at 27°C)} \quad \therefore \frac{I_e}{g_m} = \frac{I_o}{g_m} = 26mV$$

and thus for a fixed value of ω_1 the slew rate cannot be improved. It is possible to increase I_o over g_m in the bipolar process by designing the first stage with emitter degeneration (e.g. LM318) but other characteristics may be compromised; in particular V_{IO}, which requires close matching of the emitter resistors, thereby increasing the devices cost.

Using JFET input devices, in the BIFET process, the slew rates attainable are much higher because JFETS have inherently lower g_m for the same bias current. MOS transistors do provide the same slew enhancements as JFETS but greater advantages can be obtained by using a totally MOS (CMOS) structure. MOS transistors have an improved gain performance at low bias currents and process reduced circuit time constants give an inherently higher bandwidth. This reduces the required size of compensation capacitor C_c and allows a higher unity gain bandwidth frequency ω_1. The same performance as general purpose bipolar op-amps is therefore obtained at an order of magnitude less supply current. Additionally higher performance can be obtained by increasing the bias current and therefore performance can be traded against supply current. Figure 3.2 shows the a.c. and d.c. gain performance for the three supply current settings and Table 2.1 allows comparison of the other parameters.

An understanding of how the trade-offs for d.c. and a.c. performance against bias (supply) current occur within the LinCMOS process can be gained by substituting the MOS transistor parameters in the above equations with the following explanation.

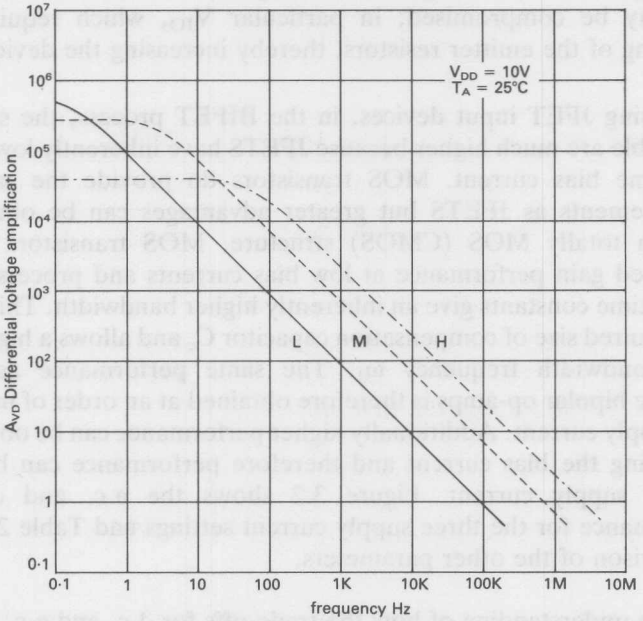
For op-amp d.c. voltage gain, $1/g_o = R_L$ is substituted in eqn (3.1) giving:

$$A_{d.c.} = \frac{g_{m1}}{g_{o1}} \times \frac{g_{m2}}{g_{o2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.6)$$

An increase in d.c. gain with decrease in bias level is shown by Figure 3.2. With the high and medium bias op-amps the MOS transistor drain current I_D levels give a d.c. voltage gain $A_{d.c.}$ (3.6) that is proportional to $1/I_D$ to a first order. This results because g_m in a MOS transistor is

proportional to $\sqrt{I_D}$ and output conductance g_o is proportional to I_D, making the ratio g_m/g_o proportional to $1/\sqrt{I_D}$.

Fig. 3.2 Large-signal differential voltage gain Vs frequency comparison for high (H) medium (M) and low (L) bias modes.



A lower increase in d.c. gain $A_{d.c.}$ (3.6) occurs from medium to low bias levels and tends to a constant value with change in I_D. This results because as drain current I_D decreases to very low levels g_m goes from being proportional to $\sqrt{I_D}$ to being directly proportional to I_D and thus the ratio g_m/g_o tends to a constant value. MOS transistors at these very low I_D levels have a bipolar type g_m and I_o relationship.

For a.c. gain the GBW product equation (3.3) remains true but as the rate of change of g_m is greater between low and medium bias than between medium and high bias, there is a correspondingly greater increase in GBW product. Slew rate is directly proportional to I_D as shown by equation (3.4).

LOW DRIFT VIO

Use of the polysilicon gate process and the careful input circuit design has given the LinCMOS operational amplifiers very good input offset voltage drift characteristics. This is shown in Table 3.1 reproduced from the data sheet. Particularly the 0.1μV/month drift figure shows how stable the process is with time.

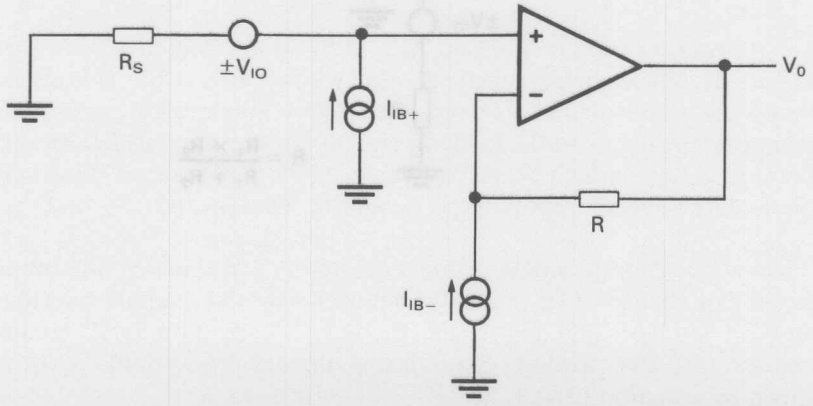
Table 3.1

Parameter Bias	Low	Medium	High
Offset voltage drift (Typ)*	0.1μV/month	0.1μV/month	0.1μV/month
Offset temp coef (Typ)	0.7μV/°C	2μV/°C	5μV/°C

*The data sheet states that these long term drift values apply after the first month. Recent characterisation has shown however that they are equally valid during the first month.

The following shows how the effects of V_{IO} drifts are calculated for the basic inverting and noninverting circuits. Contributors to the output offset are V_{IO}, $I_{IB\pm}$ and I_{IO}, where $I_{IO} = (I_{IB+} - I_{IB-})$.

Fig. 3.3 Non-inverting offset voltage and current model.



Output offset $V_o = (I_{IB+})R_s - (I_{IB-})R \pm V_{IO}$ ..... (3.7)

For matched bias resistors $R = R_s$, $V_o = \pm I_{IO}R \pm V_{IO}$ ..... (3.8)

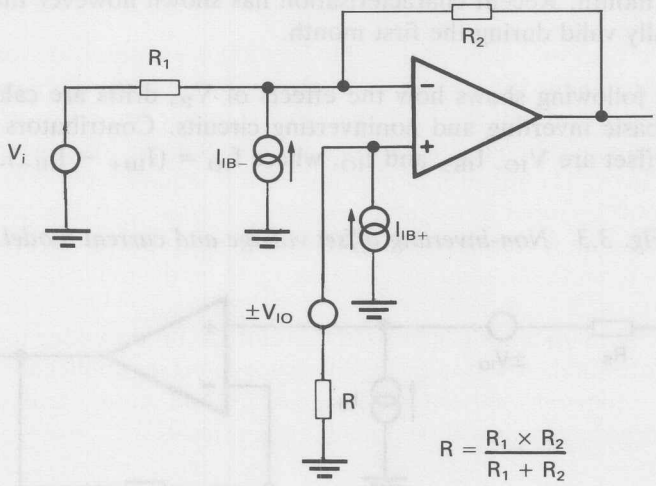
Giving temperature dependance:

$$\frac{dV_o}{dT} = \pm I_{IO}\frac{dR_s}{dT} + R_s\frac{dI_{IO}}{dT} \pm \frac{dV_{IO}}{dT} \quad \text{..... (3.9)}$$

For LinCMOS the input offset current has negligible effect except for very high values of feedback and source resistor. R needs to be >10 Mohms to give comparable offset due to I_{IO} as V_{IO}, thus ignoring terms in I_{IO}:

$$dV_o = \frac{dV_{IO}}{dT} \times dT. \qquad dV_{IO}/dT \text{ is called } \propto V_{IO} \text{ in data sheets.}$$

Fig. 3.4 Inverting offset voltage and current model.



For the circuit of Figure 3.4 assuming $V_i = 0$:

$$V_o = \pm V_{IO}\left(1 + \frac{R_2}{R_1}\right) + (I_{IB+})R\left(1 + \frac{R_2}{R_1}\right) - (I_{IB-})R_2 \quad (3.10)$$

For matched bias current resistors i.e. $R = (R_1R_2)/(R_1 + R_2)$

$$V_o = \pm V_{IO}\left(1 + \frac{R_2}{R_1}\right) \pm I_{IO}R_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.11)$$

Giving temperature dependance:

$$\frac{dV_o}{dT} = \left(1 + \frac{R_2}{R_1}\right) \times \frac{dV_{IO}}{dT} \times dT \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.12)$$

assuming R_1 & R_2 are drift free.

Again I_{IO} may be neglected except for very high resistor values (>10 Mohm). This result shows that for an inverting amplifier the gain to input signals V_i is times −1 and to V_{IO} is times 2.

Single operational amplifiers TLC251/271 have provision for input offset adjustment by use of a 25 kohm potentiometer connected between the offset null pins with the wiper connected to $-V_{DD}$ (GND). This adjustment should not be used to compensate for other circuit error voltages. The offset null pins are used to equalise the currents in each half of the input differential amplifier. If these currents are made unequal, to compensate for other error voltages in the circuit, both the temperature and long term specifications will be degraded.

LinCMOS op-amps can be used therefore to produce long term and temperature stable low power amplifiers for interface applications. The effects of input bias current are insignificant and so any temperature dependancy they have will be equally insignificant.

Notes: 1. Very precise circuits need to be concerned with the thermoelectric potentials produced by dissimilar metals such as the copper and tin/lead solder (1 to 3μV/degC) circuit connections.

2. Matching input resistances to equalise the d.c. input offset due to the bias current will not give the best a.c. noise performance. At the levels of source and feedback resistance that give resistor noise levels

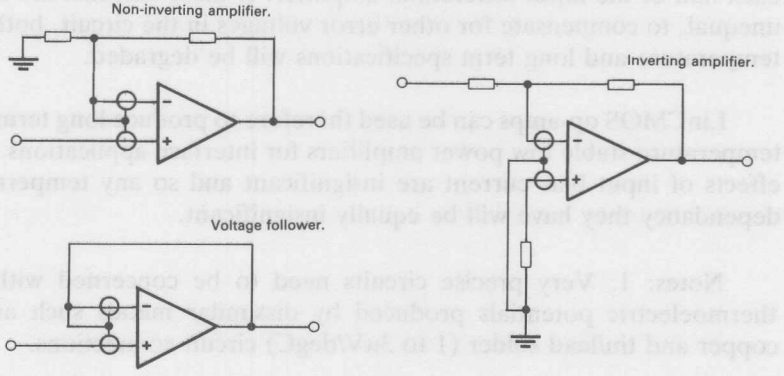
comparable with voltage input noise (e_n), the d.c. offsets due to bias current compared with V_{IO} will be small. Thus input resistors matching should not be included for best a.c. noise performance (see noise section).

LOW INPUT BIAS AND OFFSET CURRENT

PMOS input transistors have very high input impedance and potentially non-existent input currents. Practice dictates the inclusion of ESD protection circuits which still give LinCMOS op-amps an order of magnitude less bias current than BIFETs over temperature (see Table 2.1). For the above non-inverting stage a source resistor R_s of 10Mohms still only gives an offset due to I_{IO} (300 pA) equal to V_{IO} (3mV). If offset is not an important parameter much higher resistor values can be used if this is within a.c. noise constraints.

Use of high value feedback resistors has several advantages: it takes full use of the low-power capabilities, it allows the use of smaller lower cost and more precise capacitors in filter and timing circuits and it reduces the loading on the output stage allowing a wider output voltage swing.

Fig. 3.5 Guard ring schemes.



However there are precautions that have to be observed with the use of high value feedback resistors:

Leakage currents on printed circuit boards can cause problems. It is good practice to include guard rings around inputs in the form of a track on the PCB that encloses the input pins. These should be driven from a low impedance source at the same voltage as the inputs, Figure 3.5 shows three common schemes.

The input capacity of the device and strays can cause feedback poles and excess phase shift and thus stability problems. These effects can be minimised by keeping the feedback resistor connections as close as possible to the input pins and by the use of small value feedback capacitors (see stability section).

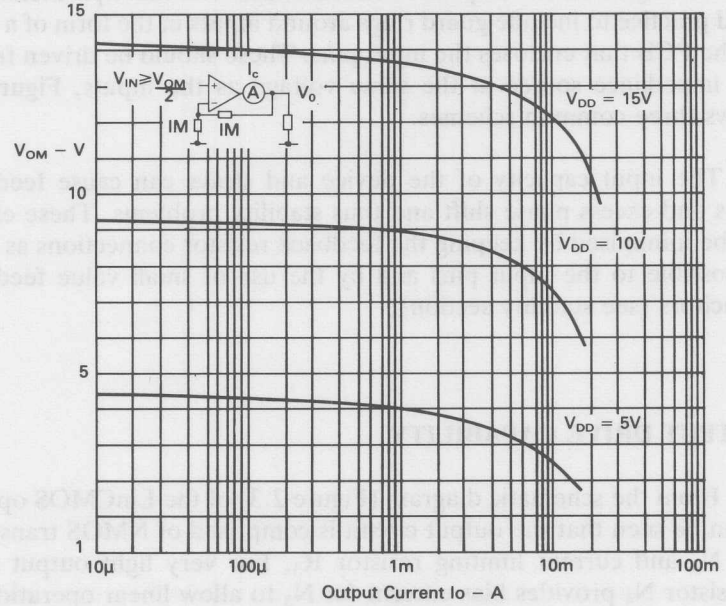
OUTPUT DRIVE CAPABILITY

From the schematic diagram (Figure 2.3) of the LinCMOS op-amp it can be seen that the output circuit is comprised of NMOS transistors N_4, N_5 and current limiting resistor R_3. For very light output loads transistor N_4 provides bias current for N_5 to allow linear operation.

Although the LinCMOS op-amp will operate with +/− supply rails it's output stage has been optimised for single rail applications. With a load connected between the output and 0V transistor N_5 supplies the output current and N_4 pulls the output down to within a few millivolts of 0V. The voltage output swing V_{OM} extends from the supply voltage V_{DD} less N_5's V_{GS} and P_4's V_{DS} to 0V. The magnitude of N_5's V_{GS} depends on the backgate voltage between the backgate of N_5 (which is the substrate) and the source of N_5, the output. As the output voltage increases above the substrate, the V_{GS} of N_5 increases. However this still results in a V_{OM} that is a higher percent of V_{DD} for higher supply voltages V_{DD}. Typical values of V_{OM} versus output current are plotted for three values of supply voltage V_{DD} 5V, 10V and 15V in Figure 3.6.

Where greater V_{OM} is needed, such as when interfacing to A–D converters operating on 5V supplies or supplying higher output currents, it can be achieved with a pull-up circuit. The simplest of these is a resistive pull-up the value of which can be calculated as shown in Figure 3.7 and equation (3.13).

Fig. 3.6 Maximum output voltage V_{OM} Vs. output current I_0 with V_{DD} as parameter.



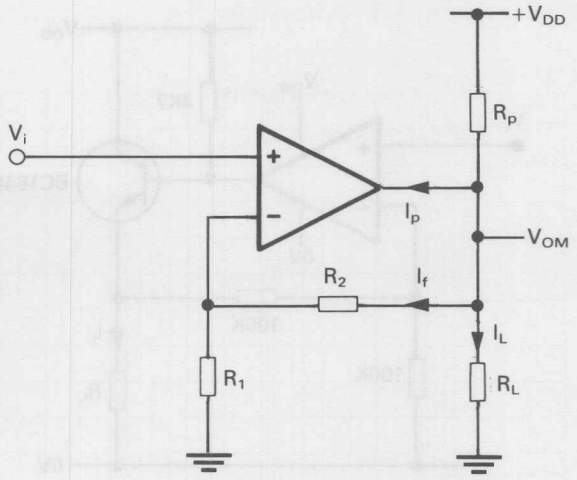
$$Rp = \frac{V_{DD} - V_{OM}}{I_f + I_L + I_p} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.13)$$

Where I_p is the pull-up current required by the op-amp, and is typically 0.5µA.

For example at V_{DD} = 5V and a required V_{OM} = 4.8V

	$R_1 = R_2$ ohms	R_L ohms	Needed R_p ohms	Sink I_o mA. due to R_p.	V_o offset from GND
(a)	1M	100k	3.9k	1.28	approx 100mV
(b)	100k	10k	390	12.8	approx 1V

Fig. 3.7 Resistive pull-up R_p.

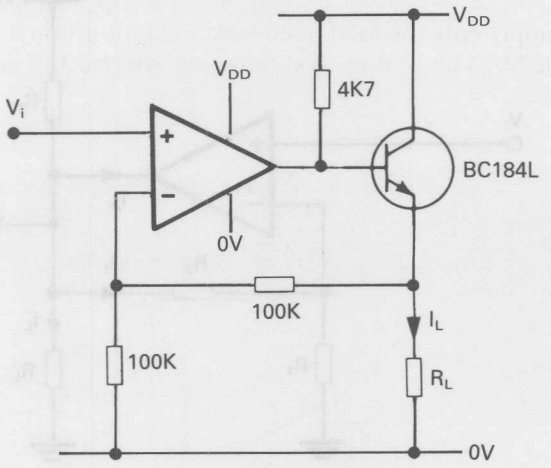


There are two disadvantages to using a simple resistive pull-up. Firstly pull-down transistor N_4 has to sink a comparatively large current. N_4 behaves like a linear resistor in this situation with an on resistance between 60–180 ohms depending on how hard the input to the op-amp is driven. With very low values of pull-up resistor a voltage offset from 0V at the output will occur. Secondly the pull-up resistor acts as a drain load to transistor N_4 and the gain of the op-amp is reduced at Vout levels where N_5 is not supplying the output current. A load of 1kohm will reduce the gain of the op-amp to approximately 3500. This effect is also observed when in dual supply operation using low load values on negative output swings.

An improved pull-up can use an emitter follower to supply a larger load current and bring the V_{OM} to within approximately 0.8 volts of the positive supply. Figure 3.8 shows a circuit for single rail application.

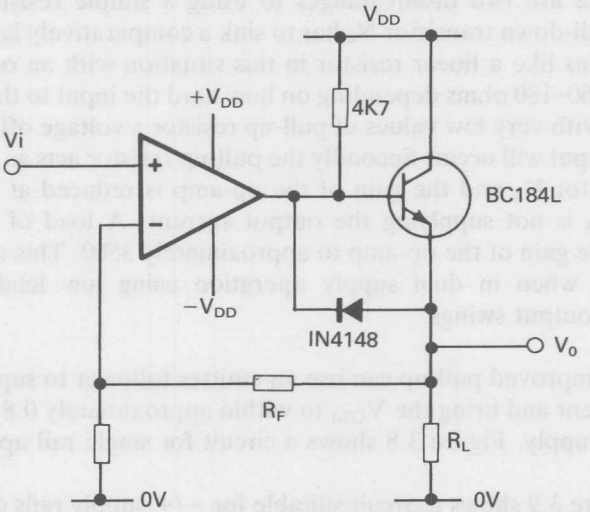
Figure 3.9 shows a circuit suitable for −/+ supply rails d.c. and low frequency applications. The speed at which the circuit will operate is dependent upon the rate the op-amp output voltage will slew across the transistor and diode offset voltages.

Fig. 3.8 Single rail load current boost circuit.



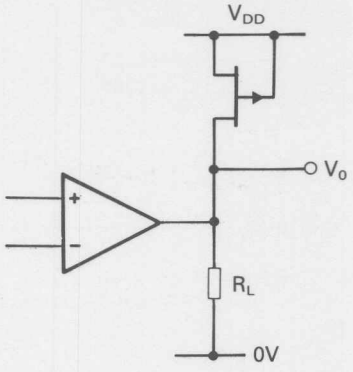
typ I_L = 20mA @ 4V output
= 5mA @ 4.2V output

Fig. 3.9 ± supply load current boost circuit.



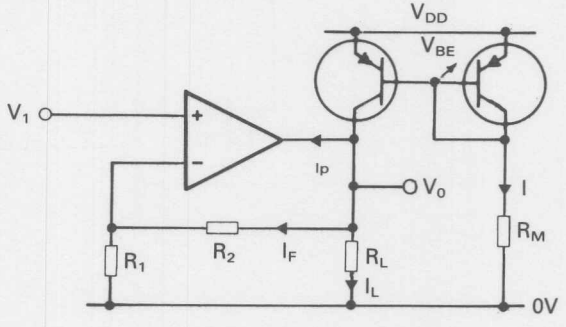
Another alternative is to use a p-channel depletion mode FET as a current source as shown in Figure 3.10. Optimally the FET chosen would supply only the load, feedback and pull-up currents at the highest operating V_{OM} and saturate at that value so that the pull-down offset is minimised.

Fig. 3.10 P channel FET pull-up.



A more successful pull-up circuit which allows the pull-up current to be defined at the optimal value employs two pnp transistors in a current mirror configuration as shown in Figure 3.11.

Fig. 3.11 Current mirror pull-up.



$$\text{Thus } I = \frac{V_{DD} - V_{be}}{R_m} = I_p + I_f + I_L \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.14)$$

For V_{DD} = 5V, required V_{OM} = 4.8V, $R_1 = R_2$ = 100k & R_L = 10k then R_m = 8.2k.

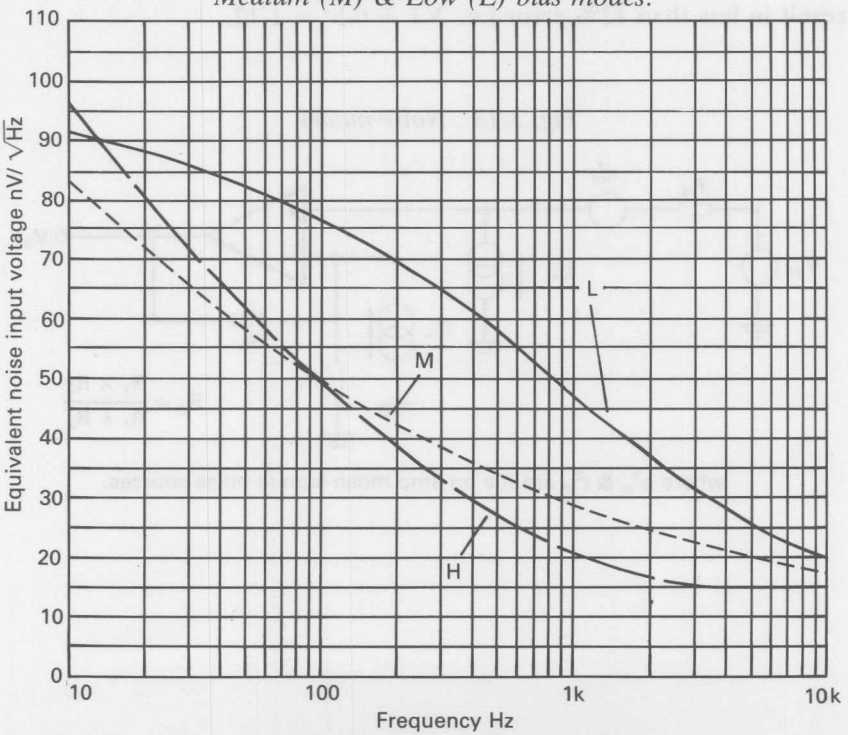
LinCMOS NOISE PERFORMANCE

Introduction

Noise performance of a system is determined by the first stages in the circuit. For an audio or video system where human perception uses the signal to mask the noise this is usually expressed in terms of signal to noise ratio or noise figure. For an analogue to digital conversion process noise determines the ultimate resolution achievable and should generally be less than the least significant bit (LSB). (There are digital filtering techniques that use noise to improve system performance by reduction of quantisation error.) The lower limit to dynamic range is set by the noise floor in any system, this includes analogue circuit noise and, in any analogue to digital conversion, the quantisation noise.

The LinCMOS op-amp typical noise voltage performance for the three supply current versions is shown in Figure 3.12.

Fig. 3.12 Equivalent input noise Vs. frequency for High (H), Medium (M) & Low (L) bias modes.

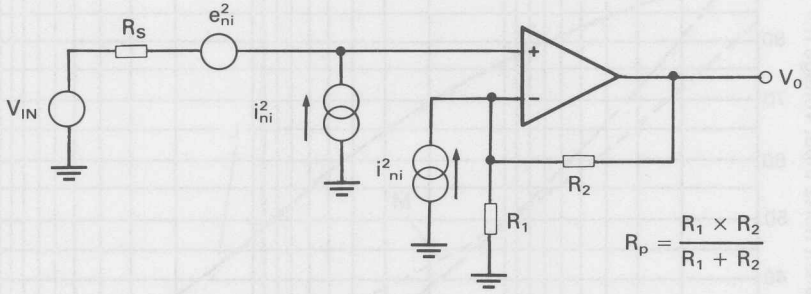


Low input bias currents of the PMOS input transistors give a very low noise current which is usually insignificant and need not be considered. This is shown to greatest advantage when using higher values of circuit impedances (greater than 50kohms). Bipolar op-amps have higher bias and noise currents which dominate the noise performance as circuit resistances are increased. It will be seen below that much higher resistor values can be used compared with bipolar for a similar noise performance which is then dominated by resistor noise.

Noise Design Steps

Initially all noise sources have to be identified and an estimation made of whether each source is significant to noise calculations. See the equivalent circuit Figure 3.13 for a non-inverting op-amp. As the noise signals in the equivalent circuit appear at the non-inverting input noise gain is always that of a non-inverting amplifier. Signal gain is dependent on where the signal is applied. RMS addition is used with uncorrelated noise sources and any noise that is less than 1/2 of the largest noise will result in less than 12% error i.e. $\sqrt{1 + 0.5^2} = 1.12$.

Fig. 3.13 Noise model.



where e^2_{ni} & i^2_{ni} are the op-amp mean-square noise sources.

The noise sources are:

(i) The equivalent op-amp noise voltage source e_{ni} in $V/\sqrt{Hz}$

(ii) Johnson noise due to source (R_s)

and feedback resistors (R_p): $e_{nR} = \sqrt{4KTRB}$ ..... (3.15)

where $K = 1.38 \times 10^{-23}$ Boltzmans constant in Joules

$T = 298°K$ (25°C)

B = Bandwidth

R = effective resistance.

Giving $e_{nR} = 0.1283nV \times \sqrt{R}/\sqrt{Hz}$. ..... (3.16)

(iii) Shot noise due to input bias current:

$i_{ni} = \sqrt{2qI_BB}$ Amps/$\sqrt{Hz}$ ..... (3.17)

($q = 1.6 \times 10^{-19}$ coulombs)

Hence the total noise referred to the non-inverting input is:

$$e_{ntot} = [e_{ni}^2 + e_{nRs}^2 + e_{nRp}^2 + i_{ni}^2 (R_s^2 + R_p^2)]^{1/2} \text{ ..... (3.18)}$$

where $R_p = \dfrac{R_1R_2}{R_1 + R_2}$

For example if $R_s = R_1 = R_2 = 100$kohms in the above circuit the equivalent noise voltage from each source is:

$e_{ni} = 38nV/\sqrt{Hz}$ for the Medium bias LinCMOS op-amp @ 1kHz.

$e_{nRp} = 28.7nV/\sqrt{Hz}$ and $e_{nRs} = 40nV/\sqrt{Hz}$

$[i_{ni}^2 (R_p^2 + R_s^2)]^{1/2} = 1.5nV/\sqrt{Hz}$ calculated using an input noise current of 13.86 fA/$\sqrt{Hz}$ (from a bias current of 600pA). This value of noise voltage is insignificant when compared with e_{ni} and e_{nRs}. The total noise equivalent voltage at the input is 62nV/$\sqrt{Hz}$.

Using the same resistor values in a circuit employing the 741 with typical e_{ni} = 22nV/$\sqrt{Hz}$ and i_{ni} = 0.55pA/$\sqrt{Hz}$ the equivalent noise voltage due noise current is 61.5nV/$\sqrt{Hz}$. This level of noise current makes a significant contribution and gives a total noise voltage of 82nV/$\sqrt{Hz}$.

For comparison if the resistor values above are increased to 1Mohm then the following results are obtained:

e_{nRp} = 90nV/$\sqrt{Hz}$ and e_{nRs} = 128nV/$\sqrt{Hz}$

Equivalent noise voltage due to input current becomes 15.5nV/$\sqrt{Hz}$ for LinCMOS and 615nV/$\sqrt{Hz}$ for the μA741.

This illustrates that, for LinCMOS, noise due to noise current is insignificant but is instead dominated by input noise voltage e_{ni} and source resistance. For the bipolar device however, the noise current is dominant.

In practice both amplifier transfer functions and noise spectral density are functions of frequency. These transfer functions include the finite bandwidth and skirt response of filters and equalisers. The noise spectral density includes flicker (1/f) with the flat thermal noise. These effects necessitate determining the equivalent "brickwall" noise bandwidth from the transfer function and then making a summation of the mean square noise voltage over this bandwidth.

The noise bandwidth is called the Noise Equivalent Bandwidth (N.E.B.) and is derived by considering the rms noise from an amplifier of gain A with transfer function H(f) and total mean square noise e_{ntot}^2 as follows:

$$Vn = [\int_0^{\alpha} e_{ntot}^2 \times A^2 \times |H(f)|^2 \times df]^{1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.19)$$

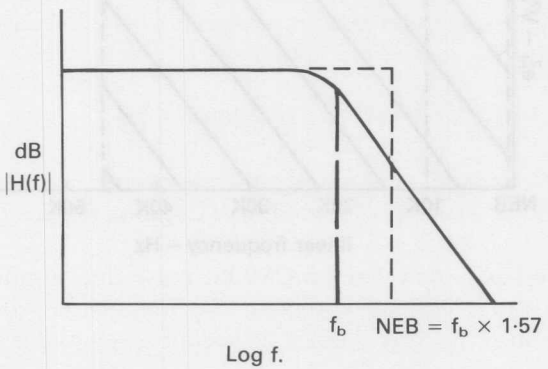
assuming constant spectral density for e_{ntot}^2

$$Vn = e_{ntot} \times A \times [\int_o^{\alpha} |H(f)|^2 \times df]^{1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.20)$$

$$N.E.B. = \int_o^{\alpha} |H(f)|^2 \times df \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.21)$$

This is shown in Figure 3.14 for a 1 pole filter with break frequency f_b whose N.E.B. is $f_b \times 1.57$ $(\pi/2)$Hz.

Fig. 3.14 Noise equivalent bandwidth.



In simple cases the N.E.B. of a transfer function or circuit impedance may be evaluated algebraically but in more complicated cases it is best evaluated numerically with the aid of a numerical integration routine.

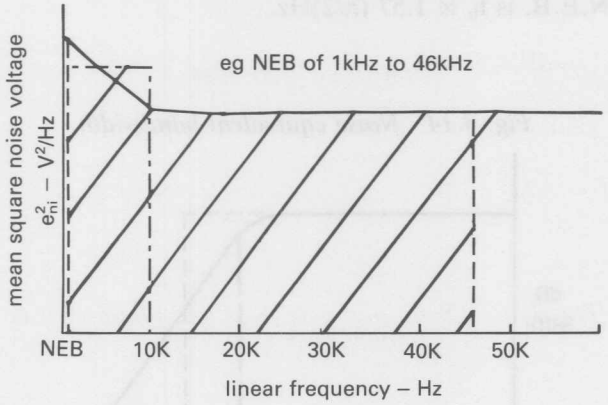
Thus the rms noise output of an amplifier is:

$$Vn = \sqrt{e_{ntot}{}^2(f)} \times \sqrt{N.E.B.} \times A \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.22)$$

where $A = 1 + \dfrac{R_2}{R_1}$ for both inverting and non-inverting configurations as the noise appears directly as an input to the non-inverting input of the op-amp.

A graphical method can be used to include the frequency dependent effects of noise spectral density. The first step is to make a sum at decade or less frequency intervals of the mean square voltage/Hz contribution of each noise source. Then a straight line graph of mean square noise voltage/Hz versus frequency is plotted on linear scales. The mean square noise voltage over the N.E.B. is calculated by a summation of the values of mean trapezoidal heights times the corresponding base line. Figure 3.15 shows an example.

Fig. 3.15 Mean square noise summation example.



STABILITY

Stability of a negative feedback amplifier is dependent on the loop phase shift and gain characteristics. That is, the gain and phase shift of the amplifier and feedback network in cascade. This is commonly expressed as phase margin and is the amount by which the excess phase shift due to the amplifier and feedback network is less than 180° when the loop gain is unity. Excess phase shift is the additional phase shift in the loop over the 180° due to negative feedback.

Bode plots of open loop gain, on a log (dB) scale, and phase shift versus log frequency are plotted on data sheets and are typically shown in Figure 3.16 for the LinCMOS TLC271 (high bias). By plotting the closed loop gain on the Bode plot, as shown, the frequency where loop gain ($A_{OL}\beta$) equals unity gives the operating phase margin on the corresponding phase shift plot. Thus in general phase margin can be determined for any value of closed loop gain at loop gain equal to unity. Phase margin is quoted in data sheets at the worst case which is when closed loop gain is unity (voltage follower configuration). Although the gain versus frequency Bode plot does not show higher order frequency roll off effects, these are indicated on the phase shift plots as small contributions to the excess phase. Using these plots and the standard equations shown for a feedback amplifiers much can be understood about an op-amps a.c. performance.

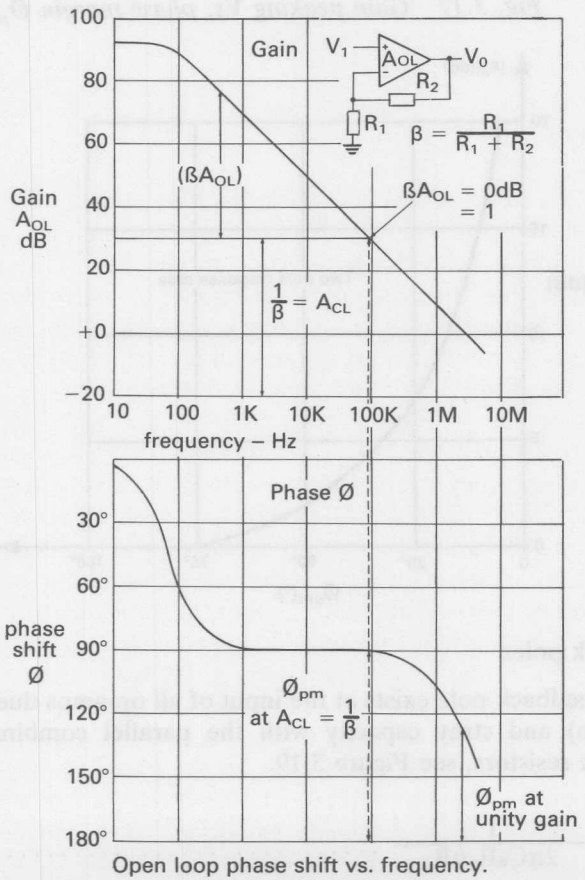
$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.22)$$

Expressed in dB's. For $A_{OL} >> 1$ where $A_{CL} = 1/\beta$

loop gain = open loop gain − closed loop gain

$$A_{OL}\beta = A_{OL} - 1/\beta \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.23)$$

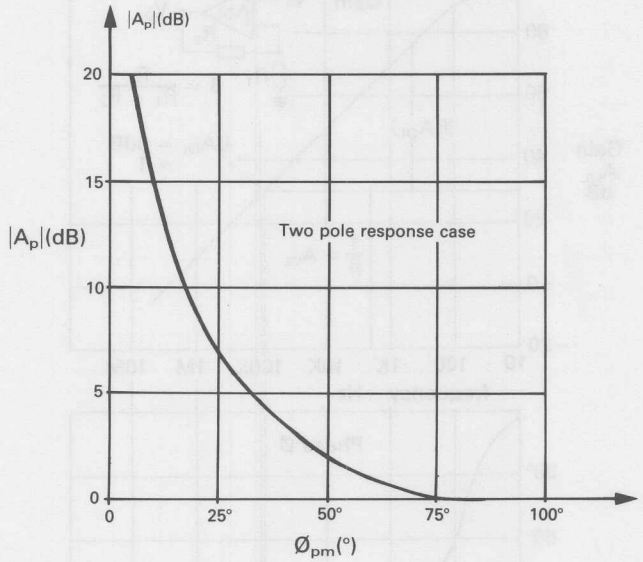
Fig. 3.16 Open loop gain A_{OL} and phase shift Ø Vs. frequency (TLC271 'H').



Open loop phase shift vs. frequency.

A typical response of an op-amp internally compensated for unity gain operation is shown in Figure 3.16. Op-amps of this type have one break frequency (pole) positioned at a low frequency to dominate the phase response versus frequency to ensure stability at unity gain with an acceptable phase margin. The total excess phase at unity gain will be the 90° due to the compensation pole plus additional phase shift from other high frequency poles within the op-amp. Total loop ($A_{OL}\beta$) excess phase shift of less than 180° but more than 90° will cause some peaking of the closed loop gain response at the bandwidth limit. Associated with this will be overshoot and ringing in the transient response. Figure 3.17 shows a graph of gain peaking versus phase margin and Figure 3.18 shows transient response.

Fig. 3.17 Gain peaking Vs. phase margin $\emptyset_{pm}$.



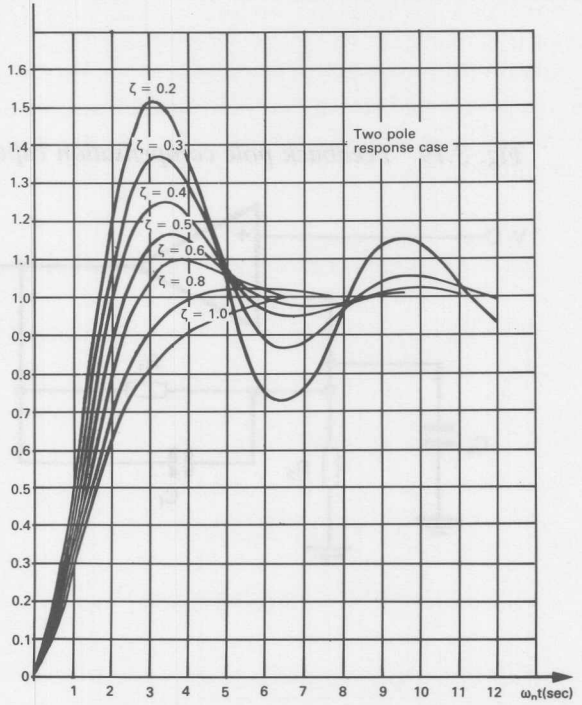
Feedback poles

A feedback pole exists at the input of all op-amps due to the input (5pF typ) and stray capacity with the parallel combination of the feedback resistors, see Figure 3.19.

$$f_c = \frac{1}{2\pi C_S R_1 // R_2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.24)$$

Fig. 3.18 Transient response Vs. damping factor.

$$\zeta = \sqrt{\frac{1}{\frac{\text{Cos } \emptyset_{pm}}{\text{Sin}^2 \emptyset_{pm}}}}$$ gives relationship between phase margin $\emptyset_{pm}$ & ζ



$$\phi = \tan^{-1}\left(\frac{f}{f_c}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.25)$$

There is more likelihood of the feedback pole making a significant contribution to excess phase shift, and thus causing instability, using low power circuits with high values of feedback resistors (100k's) than with the more usual 10k's of bipolar op-amps. The phase contribution can be calculated from equation (3.25) above using the cut off frequency from (3.24), f is the frequency where the loop gain is unity. Values for f/fc = 6 are 10° and f/fc = 10 are 5.7°.

Practical solutions to this problem are to minimise the stray capacitance by making the resistor connections physically close to the IC pins and, where necessary, add a feedback capacitor C_f as shown in Figure 3.19. The value of C_f should be $\leq(R_2C_s)/R_1$ Larger values of C_f can be used to improve the phase margin and reduce gain peaking. This also reduces the bandwidth which can be useful in reducing noise.

Fig. 3.19 Feedback pole compensation capacity C_f.

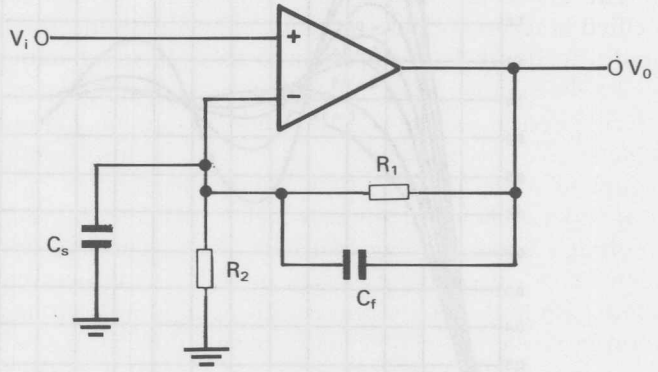
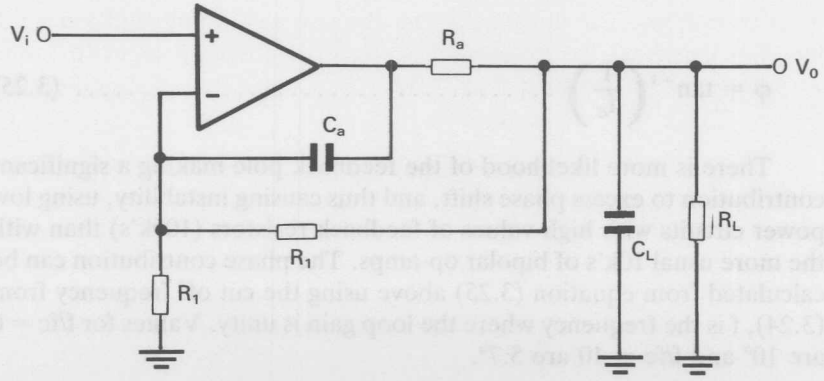


Fig. 3.20 Output pole compensation capacitor C_a and resistor R_a.



Output poles

A pole exists at the output of an op-amp as a result of the op-amp's output resistance and the load capacitance and can be a cause of instability due to the excess phase introduced. One source of load capacity are cables, which are entirely capacitive for lengths much shorter than a wavelength. The LinCMOS devices are specified with 100pF load capacitance. The above equations allow the calculation of the excess phase contribution as for the feedback pole. A circuit solution to the problem of high capacitive loads is shown in Figure 3.20. The values for R_a and C_a are best determined empirically.

The above description has outlined the way op-amp stability is specified in terms of phase margin and how the concept of excess phase round a feedback loop can be used to understand stability problems. This has been concerned only with circuit constraints and has assumed perfect physical circuit layout and decoupling. However stability problems are often encountered because of insufficient or incorrect decoupling, or because the connection of components to ground is in the wrong order. When designing analogue circuits there is no substitute for a thorough understanding of where circuit currents flow. From this understanding decoupling can be provided to aid current flow in the correct path and thereby prevent instability. Also ground connections should be made to prevent load currents flowing in small signal input circuits, causing instability or more subtly a performance degradation in the form of d.c. errors or a.c. distortion.

Care should be exercised in the value and type of capacitors chosen for decoupling. Wiring at the higher frequency end of an op-amp's range can present enough inductance to resonate with small value decoupling capacitors. This is cured by larger values or by inclusion of small values of series resistor. The message is that the perfect (infinite sink) ground does not exist and the unthoughtful use of decoupling capacitors can cause more problems than they solve.

ELECTROSTATIC DISCHARGE PROTECTION

All semiconductor devices, MOS and Bipolar, are susceptible to electrostatic discharge (ESD) at some level: most are ESD sensitive at 2kV or less. Greater attention has been paid to this subject with the introduction of MOS memories and CMOS logic, and LinCMOS shares in the development work that has taken place to reduce the sensitivity of these devices to ESD. Improvements in ESD thresholds are continuously being made in all these product areas but these will not be able to achieve the sort of levels that can be encountered in uncontrolled and careless handling of devices. To ensure the performance of devices is maintained, good handling and packaging practices should always be observed. (Contact T.I. Customer Response Centre for further information.)

CMOS devices are voltage sensitive due to the basic input structure consisting of a dielectric between two conductive layers that can be destroyed by an electric field of about 60V. This dielectric is protected by an input circuit which consists of diodes, zeners, resistors and thickfield MOS transistors. Outputs also need to be protected and this is achieved using small value resistors and thickfield MOS transistors.

The protection circuits cause the input bias currents to be temperature dependent and have the characteristic of a reversed bias diode within the values quoted in the data sheet.

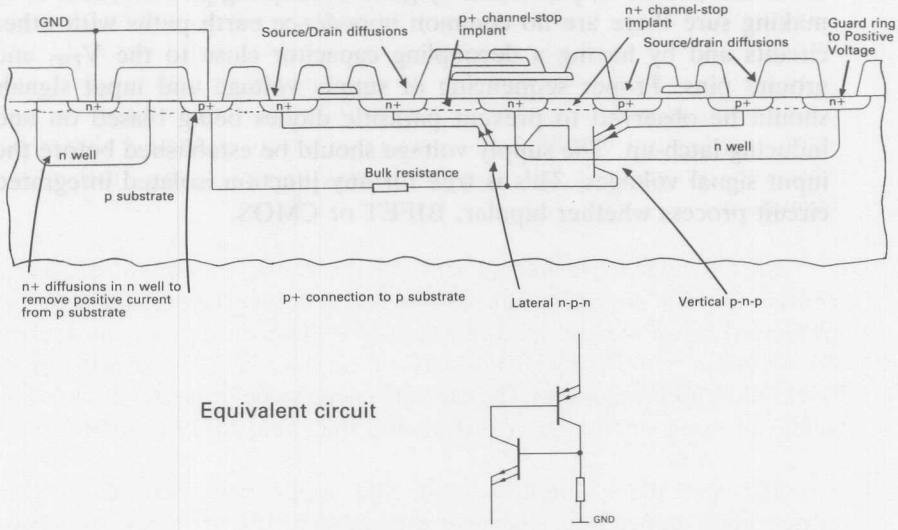
These circuits will prevent catastrophic failure when tested with voltages up to 2kV according to MIL STD 883B method 3015.1. This test specifies 5 discharges at one second intervals of a 100pF capacitor at 2kV through a 1.5kohm resistor into each terminal. The data sheet warning of parametric degradation after such a test substantially refers to an increase of input bias current I_{IB} to low tens of nano-amps.

LATCH-UP

Latch-up is the uncontrolled flow of current through the parasitic thyristors inherent in all CMOS devices (see Fig. 3.21). The current path is generally between the V_{DD} and ground pins of the IC and can be triggered by excessive currents in the signal pins or by di/dt stress of the V_{DD} pin. Once the thyristor is triggered, the current flow is limited only by the impedance of the power supply and the forward resistance of

these thyristors. This can result in the destruction of the device. Latch-up is more likely to occur at high supply voltages and temperatures.

Fig. 3.21 Latch-up mechanism, & prevention.



Conditions permitting latch-up exist whenever the gain product of the parasitic n-p-n and p-n-p transistors forming the thyristor exceeds unity. In the LinCMOS N−well process a vertical p-n-p is formed by the P+source/drain, N− well and P− substrate and a lateral n-p-n is formed by the N+source/drain, P− substrate and N− well. This N−well configuration gives the minimum gain for these transistors. The parasitic thyristor is triggered by bulk currents in the substrate.

To minimise the chance of latch-up, extra diffusions regions are introduced which shunt current out of the substrate and away from the bases of the parasitic transistors. This is achieved in LinCMOS by the use of N+ guard rings around all N−well edges with P+ guard rings around particularly sensitive structures. The LinCMOS devices are tested to ensure latch-up does not occur with −100mA drawn from any pin with normal supply voltages.

Application circuits should be designed to prevent latch-up inducing currents being injected into the substrate. ESD protection diodes should not by design be forward biased. This is achieved by not allowing input and output voltages to go more than 0.3V beyond either supply rail. For this reason care should be used when capacitively coupling pulse generators and using capacitors in pulse circuits. Supply transients should be prevented by good decoupling practice; that is by making sure there are no common impedance earth paths with other circuits and by having a decoupling capacitor close to the V_{DD} and ground pins. Proper sequencing of supply voltage and input signals should be observed to prevent parasitic diodes being biased on and inducing latch-up. The supply voltage should be established before the input signal voltages. This is true for any junction isolated integrated circuit process whether bipolar, BIFET or CMOS.

4. Applications Section

INTRODUCTION

This section contains some application examples for op-amps with particular reference to the LinCMOS TLC27__/25__ range. No claim is made for the circuits' originality but rather they appear as an aid to memory. Most have some circuit analysis to illuminate operation and stimulate further user ideas.

As described in the previous section, the LinCMOS op-amp's low input bias performance eliminates the need for bias compensation resistors thus simplifying circuits. Most circuits indicate how they should be biased for single supply operation to take advantage of the common mode range to GND ($-V_{DD}$) performance. This is indicated by a V_b rail which for single rail operation is a bias voltage and for +/− supply rails the usual GND (0V). Bias voltage can be most often derived by using a simple resistive divider, but to provide a low impedance source 'spare' op-amps in quads, for instance, can be utilised.

The trade-off between power and op-amp speed (gain-bandwidth product and slew rate) by selection of supply current through bias mode (H, M or L) has been described above. When making the bias mode selection careful evaluation of the bandwidth and slew rate requirements of the signal being conditioned should be made.

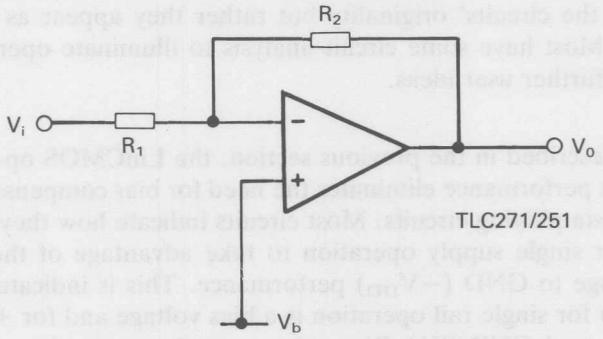
Enough bandwidth should be available so that the open loop gain exceeds the closed loop gain by a sufficient amount (i.e. 10×) at the frequencies of interest to give the required gain error or distortion performance. For specialised applications such as filters the bandwidth, and consequently the phase response, has an impact on the filters' accuracy (and sometimes stability).

Slew rate requirements are determined by the rate of change of output voltage with time given by the maximum value of $d(V_O(t)/dt$, where $V_O(t)$ is the output voltage function with time. For sinewaves ($V_{opk}.\sin\omega t$) the maximum slew rate is $\omega.V_{opk}$, and thus both frequency and signal amplitude are important. For complex feedback networks (such as filters) instability at varying output amplitude levels can be caused due to phase shifts at the onset of slew rate limiting.

AMPLIFIERS

Basic Inverting

Fig. 4.1 Basic inverting amplifier.



The expression for output voltage is given below including a bias or level shift voltage V_b which is necessary for single rail operation. The gain error term $[1 - 1/A\beta]$ is included in the equation, for very large A this tends to unity.

$$V_o = -\frac{R_2}{R_1}\left(1 - \frac{1}{A\beta}\right) V_i + V_b \quad \text{where } \beta = \frac{R_1}{R_2 + R_1}$$

hence the gain for operation around the bias level is:

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

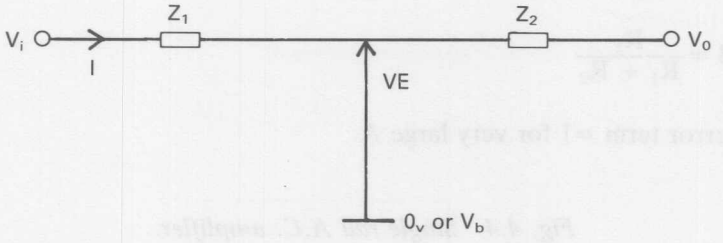
The 'virtual earth' that appears at the inverting input of the op-amp is a useful concept when calculating transfer functions thus:

For V_e referred to 0V in general $V_i = IZ_1$ & $V_o = -IZ_2$ giving

$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$

For V_e referred to V_b: $V_i - V_b = IZ_1$ & $V_o - V_b = -IZ_2$ giving

Fig. 4.2 Virtual earth diagram.



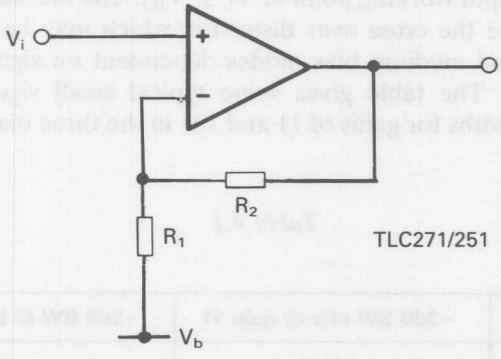
$$V_o = -\frac{Z_2}{Z_1} V_i + V_b \left(1 + \frac{R_2}{R_1}\right)$$

where R_1 & R_2 are the d.c. path of Z_1 & Z_2.

These equations give the idealised voltage gain and output, deviations such as V_{IO}, CMMR and K_{SVR} can be calculated as separate inputs to modify the 'ideal' result.

Basic Non-inverting and a.c. Amplifier

Fig. 4.3 Non-inverting amplifier.



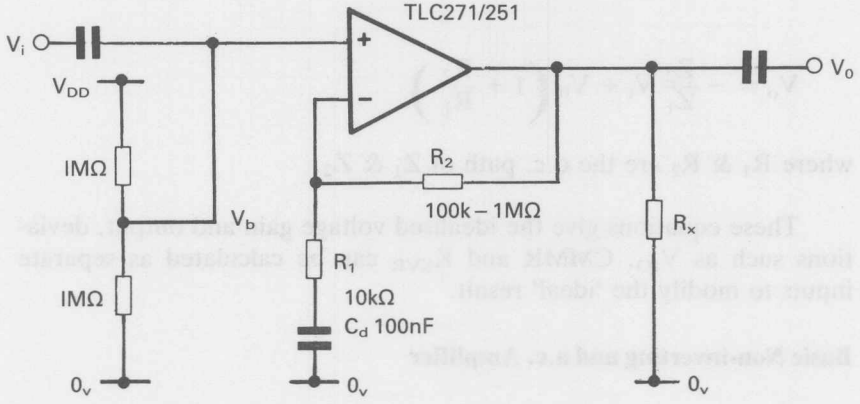
V_i is referenced to V_b.

$$V_o = \left(1 + \frac{R_2}{R_1}\right)\left(1 - \frac{1}{A\,\beta}\right) V1 + V_b$$

$$\beta = \frac{R_1}{R_1 + R_2}$$

gain error term =1 for very large A.

Fig. 4.4 Single rail A.C. amplifier.



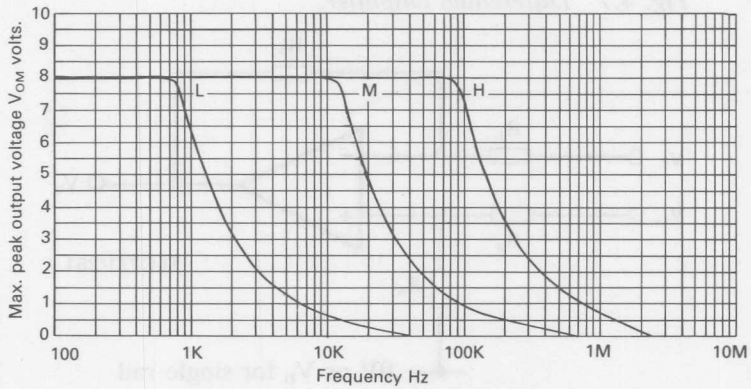
Decoupling capacitor Cd allows a high a.c. gain with unity d.c. gain keeping the output working point at $V_b \pm V_{IO}$. The inclusion of resistor Rx will improve the cross over distortion which may be encountered with the low and medium bias modes dependent on signal amplitude and frequency. The table gives some typical small signal (not slew limited) bandwidths for gains of 11 and 101 in the three bias modes with $V_{DD} = 5V$.

Table 4.1

Bias mode	−3dB BW kHz @ gain 11	−3dB BW @ kHz gain 101
Low	13.5	1.4
Medium	93.0	8.0
High	234.0	22.4

Large signal bandwidth is limited by slew rate considerations and Figure 4.5 shows typical plots for these at the three bias levels. This Figure shows that the large signal bandwidth imposes no limitations on the audio bandwidth at low values of closed loop gain for the high bias mode. The high bias mode also provides good quality audio output over this bandwidth in contrast to most bipolar single rail types.

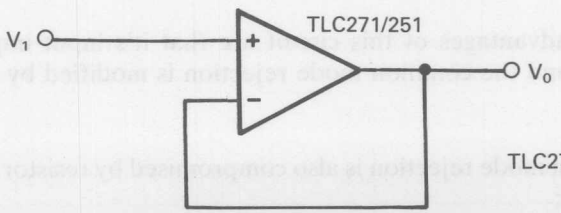
Fig. 4.5 Typical peak output voltage V_{OM} Vs. frequency.



An a.c. voltage follower is easily produced by replacing R_2 by a short circuit and removing R_1 and C_d. The low bias currents mean that high value bias resistors may be used eliminating the need for 'bootstrapping' to increase the bias circuit impedance.

Unity Gain Voltage follower.

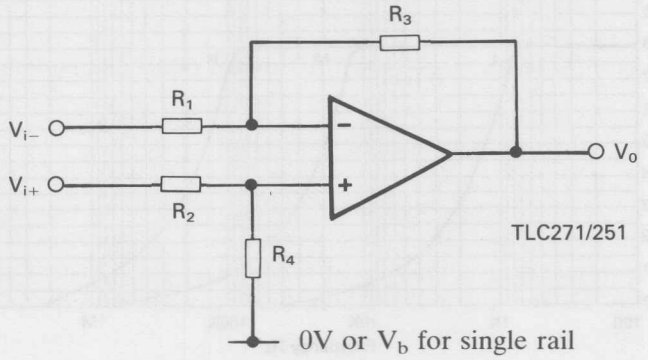
Fig. 4.6 Unity gain voltage follower.



$\frac{V_o}{V_i} = \left(1 - \frac{1}{A}\right)$ and gives 2μV/V output error in low bias mode and takes advantage of long term drift and temperature coefficient performance (0.1μV/month and 0.7μV/oC).

Differential Amplifier

Fig. 4.7 Differential amplifier.



This is the classical differential amplifier (subtractor) analysed as follows:

By superposition $V_o = \frac{R_4}{R_2 + R_4} \times \left(1 + \frac{R_3}{R_1}\right) \times V_{i+} - \frac{R_3}{R_1} \times V_{i-}$ (1)

if $R_1 = R_2$ and $R_3 = R_4$

this reduces to $V_o = (V_{i+} - V_{i-}) . \frac{R_3}{R_2}$

The disadvantages of this circuit are that it's input impedance is unbalanced and the common mode rejection is modified by the source impedances.

Common mode rejection is also compromised by resistor tolerances as illustrated:

$$\text{CMRR} = \left| \frac{\text{Differential Gain}}{\text{Common mode Gain}} \right| \text{ by definition.}$$

Substituting the common mode signal V in (1) gives common mode gain:

$$\frac{V_o}{V} = \left[\frac{R_4}{R_2 + R_4} \left(1 + \frac{R_3}{R_1} \right) - \frac{R_3}{R_2} \right]$$

substituting $R_3 = R_4 = 100\ R_1$ with $R_2 = 1.1\ R_1$ i.e. 10% mismatch gives $V_o/V = -0.099$

$$\text{therefore CMRR} = \frac{100}{0.099} = 1010 \text{ approx 60dB i.e. a nominal 20dB}$$

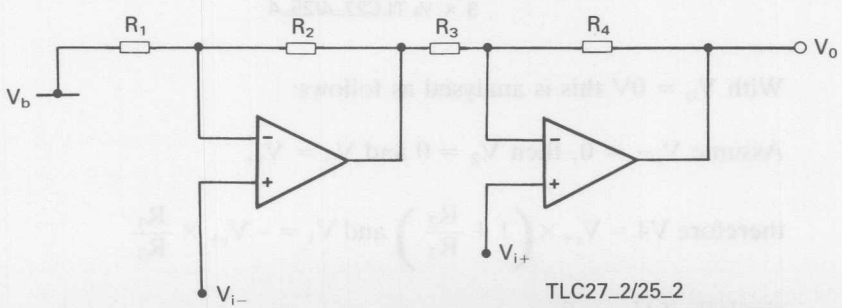
reduction in the op-amps normal specification.

Again higher values of resistance (i.e. 100kohms) can be used to implement the circuit, but a small value of capacitor across R_3 will be needed to prevent instability and overshoot in the transient response, particularly for the low and medium bias devices where phase margin degradation due to input poles has a greater effect. This circuit will operate with single rail by use of a suitably chosen bias V_b.

Two Op-amp Instrumentation Amplifier

A differential amplifier that has high and balanced input impedance and employs two op-amps (e.g. duals TLC272__/252__) is shown below:

Fig. 4.8 Two op-amp instrumentation amplifier.



By superposition:

$$V_o = \left(1 + \frac{R_4}{R_3}\right) V_{i+} - \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3} V_i \quad (\text{for } V_b = 0)$$

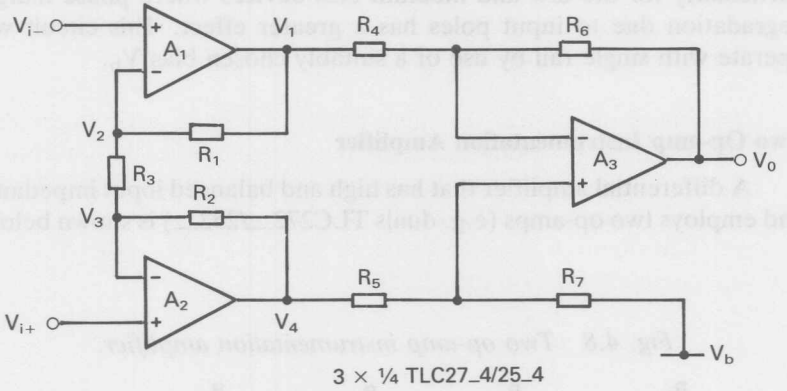
$$\text{For } R_1 = R_4 \text{ and } R_2 = R_3 \quad V_o = (V_{i+} - V_{i-}) \left(1 + \frac{R_1}{R_2}\right)$$

The circuit has the same common mode rejection performance as the previous circuit. The main limitation to performance is in CMR to a.c. signals. This is caused by the V_{i-} input being bandlimited by two op-amps as opposed to one for the V_{i+} input.

Three Op-amp Instrumentation Amplifier

This is a differential amplifier that has high input impedance and overcomes the problem of mismatched CMR to a.c. signals.

Fig. 4.9 Three op-amp instrumentation amplifier.



With $V_b = 0V$ this is analysed as follows:

Assume $V_i- = 0$, then $V_2 = 0$ and $V_3 = V_{i+}$

$$\text{therefore V4} = V_{i+} \times \left(1 + \frac{R_2}{R_3}\right) \text{ and } V_1 = -V_{i+} \times \frac{R_1}{R_3}$$

similarly if $V_{i+} = 0$

$$V_1 = V_{i-} \times \left(1 + \frac{R_1}{R_3}\right) \text{ and } V_4 = -V_{i-} \times \frac{R_2}{R_3}$$

$$\text{by superposition } (V_4 - V_1) = (V_{i+} - V_{i-}) \left(1 + \frac{R_1 + R_2}{R_3}\right)$$

if $R_6 = R_7$ and $R_4 = R_5$ then A3 functions as the basic differential amplifier and:

$$V_o = (V_{i+} - V_{i-}) \frac{R6}{R_4} \left(1 + \frac{R_1 + R_2}{R_3}\right)$$

Matching around A3 determines CMRR as described previously and differential gain can be controlled by R_3. Optimisation of CMR can be achieved by adjustment of R_7.

This amplifier can be built from a quad op-amp, TLC27_4/TLC25_4 where _ denotes bias mode. For example, if the application common mode range allowed, a really low power (8μW at 1V V_{DD}), slow speed (enough for a temperature sensor with slew rate of 0.001V/μs), high impedance interface circuit could be built using a TLC25L4. This example is at the extreme in terms of power, speed and voltage ranges but demonstrates the possibilities.

The spare op-amp in the quad package may be used to enhance circuit performance. Connected as an inverting amplifier driven from V_o it can provide more gain. Connected as a voltage source (Figure 4.10) it can be used to drive V_b without affecting common mode rejection and connected as Figure 4.11 it can be used as a shield-guard drive to reduce the capacitive effects of input cables.

Fig. 4.10 Low impedance bias voltage circuit.

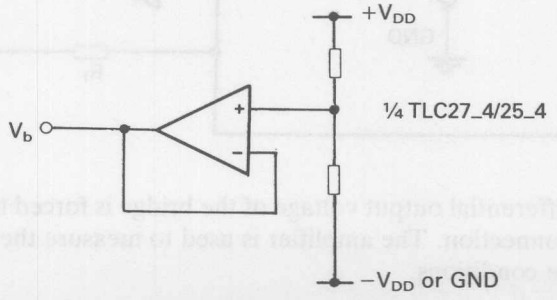
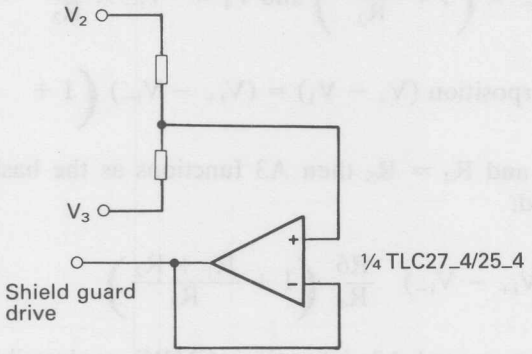


Fig. 4.11 Shield guard drive circuit.

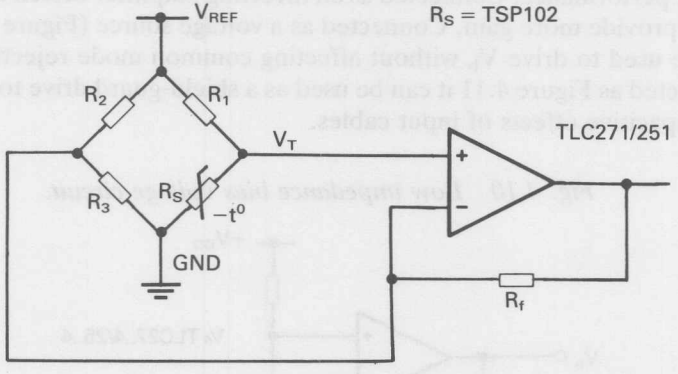


Again with higher value feedback resistors, particularly in the low and medium bias modes, small value capacitors across the feedback resistors may be necessary to ensure stability.

Bridge Amplifier

Basic circuit

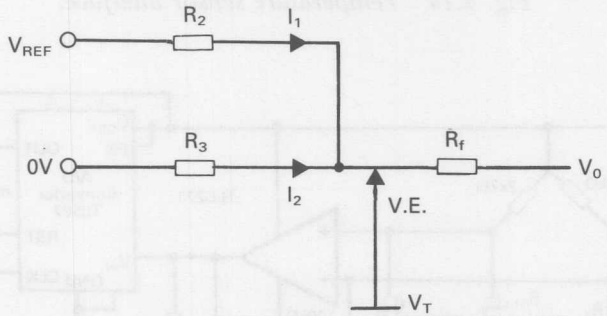
Fig. 4.12 Bridge amplifier used to sense temperature.



The differential output voltage of the bridge is forced to zero by the feedback connection. The amplifier is used to measure the current flow under these conditions.

The circuit can be analysed using 'virtual earth' analysis with the earth at potential V_T:

Fig. 4.13 Virtual earth bridge analysis.



$$V_T = \frac{V_{ref} R_s}{R_1 + R_2}$$

$$I_1 = \frac{V_{ref} - V_T}{R_2}; \quad I_2 = -\frac{V_T}{R_3}; \quad \frac{V_o - V_T}{R_f} = -(I_1 + I_2)$$

Therefore $V_o = V_T - R_f(I_1 + I_2)$

$$= V_T + R_f \cdot \left(\frac{V_T}{R_3} - \frac{V_{ref} - V_T}{R_2} \right)$$

Re-arranging for V_T and putting $R_1 = R_2 = R_3 = R$

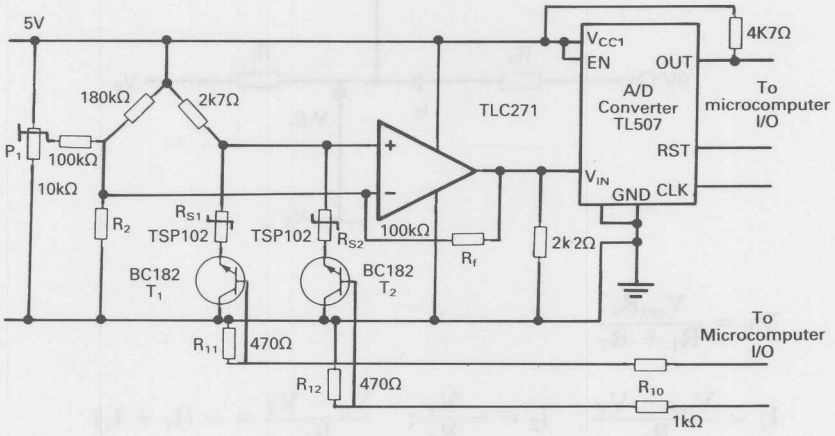
$$V_o = V_T \left(1 - \frac{2R_f}{R} \right) - \frac{V_{ref} R_f}{R}$$

substituting for V_T and $R_s = R(1 + d)$

$$V_o = V_{ref} \times \frac{R_f}{R} \times \frac{d}{1 + d} \quad \text{For } d << 1 \quad V_o = V_{ref} \times \frac{R_f}{R} \times \frac{d}{2}$$

As the input bias current of the LinCMOS op-amps are so small it is not necessary to include a resistor from (+) input to 0V. to balance input currents. Figure 4.14 shows this circuit used in a typical application.

Fig. 4.14 Temperature sensor interface.



Output Current Booster Amplifiers

Various configurations can be used to boost output current capability, three of which are shown here:

Figure 4.15 shows a single rail amplifier feeding current to a load connected to GND.

Fig. 4.15 Single rail current booster feeding to ground.

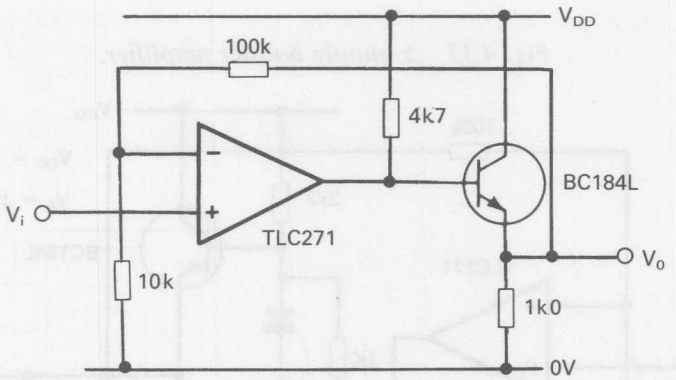


Figure 4.16 shows a single rail amplifier feeding current to a load connected to V_{DD}.

Fig. 4.16 Single rail current booster feeding to $+V_{DD}$.

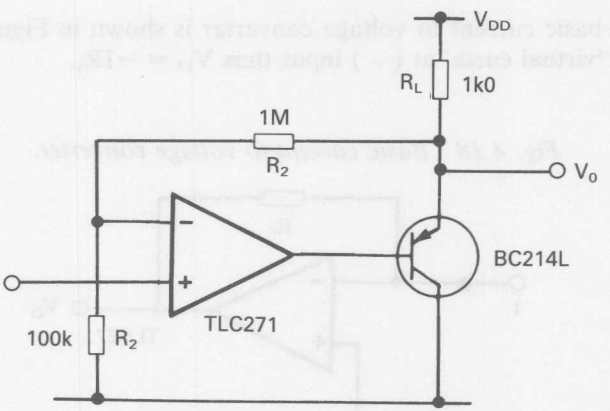
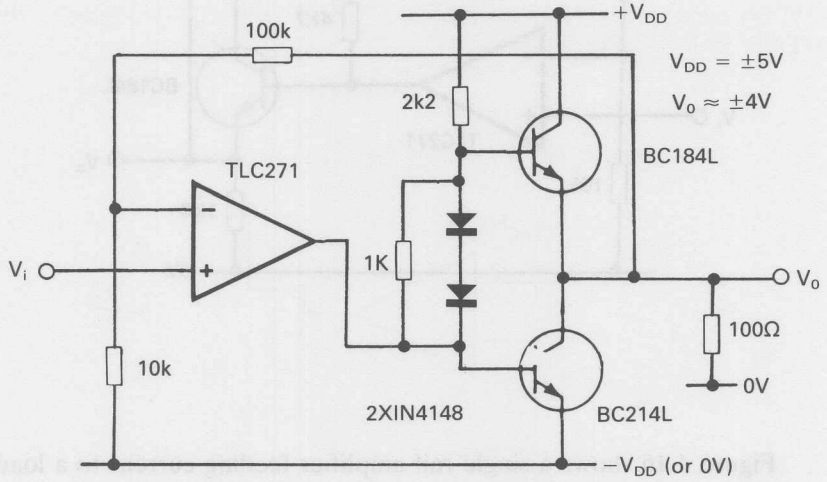


Figure 4.17 shows a +/− supply rail amplifier.

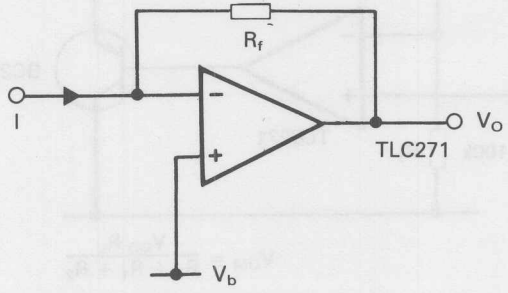
Fig. 4.17 ± supply booster amplifier.



Current Amplifiers

The basic current to voltage converter is shown in Figure 4.18 R_f causes a 'virtual earth' at (−) input thus $V_O = -IR_f$.

Fig. 4.18 Basic current to voltage converter.



Current Sink

Low op-amp bias current and low V_{IO} selections (AC = 5mV max. & BC = 3mV max.) allow precision low current sink circuits as shown in Figure 4.19. The common mode range to 0V on the inputs allows wide control range. Figure 4.20 shows a circuit for larger current sink capability.

Fig. 4.19 Precision low current sink.

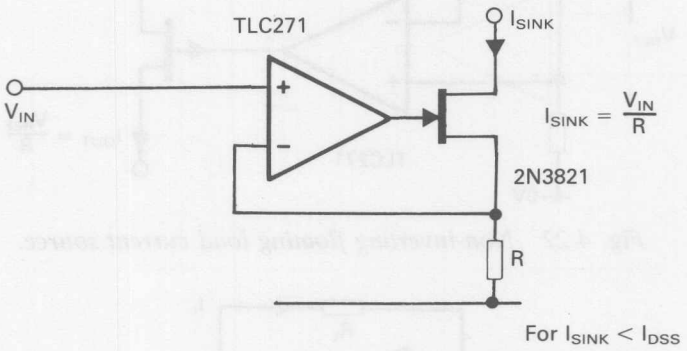
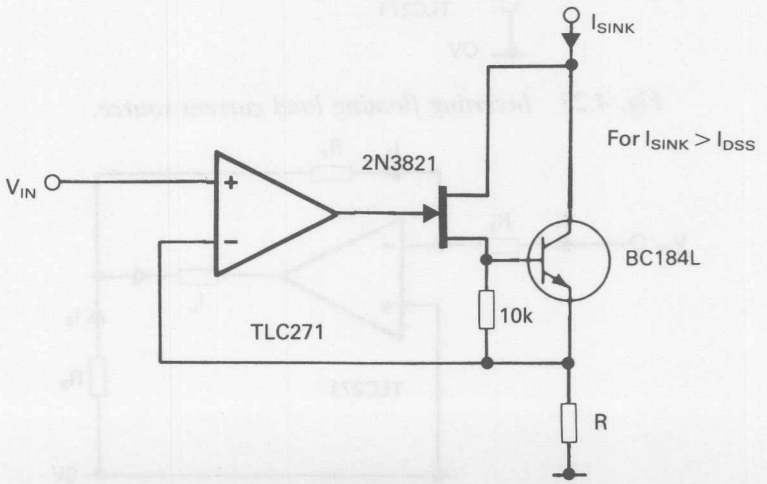


Fig. 4.20 Higher current sink.



Current Source

Figures 4.21 to 4.24 show four different configuration of current source.

Fig. 4.21 Positive current source.

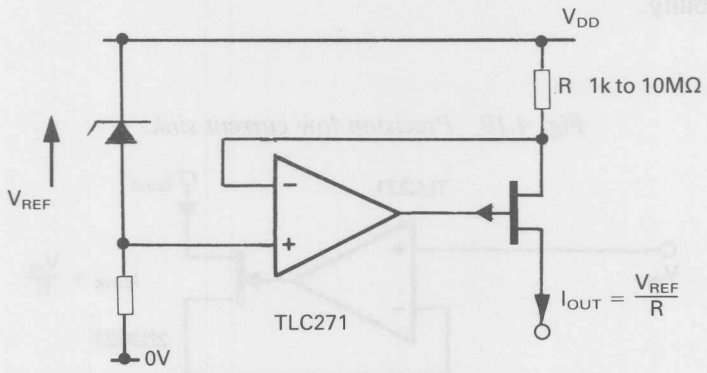


Fig. 4.22 Non-inverting floating load current source.

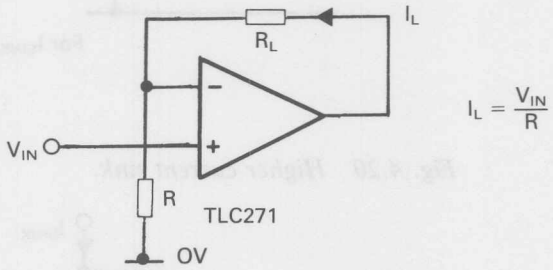
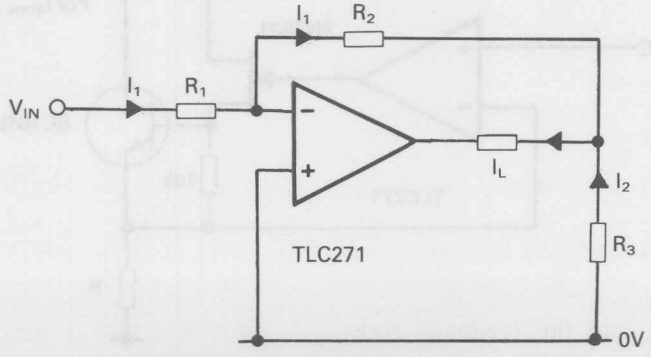


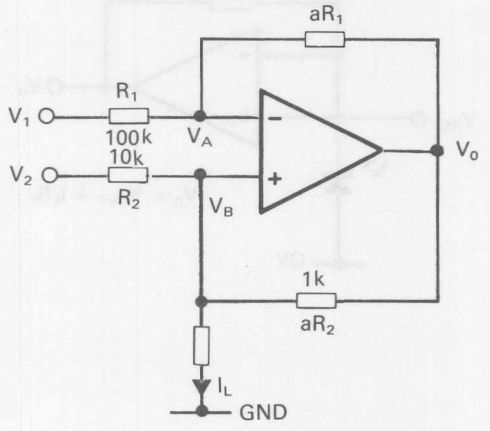
Fig. 4.23 Inverting floating load current source.



$$I_1R_2 = I_2R_3 \;\&\; I_1 = \frac{V_{in}}{R_1}$$

$$\therefore I_L = I_1 + I_2 = I_1\left(1 + \frac{R_2}{R_3}\right) = \frac{V_{in}}{R_1}\left(1 + \frac{R_2}{R_3}\right)$$

Fig. 4.24 Earthed load current source.



$$\frac{V_1 - V_A}{R_1} = \frac{V_A - V_o}{aR_1} \quad \therefore V_o = V_A(1 + a) - aV_1$$

$$\therefore I_L = \frac{V_2 - V_B}{R_2} + \frac{V_o - V_B}{aR_2}$$

$$= \frac{V_2 - V_B}{R_2} + \frac{V_A(1 + a) - aV_1 - V_B}{aR_2}$$

but $V_A = V_B \therefore I_L = \dfrac{V_2 - V_1}{R_2}$

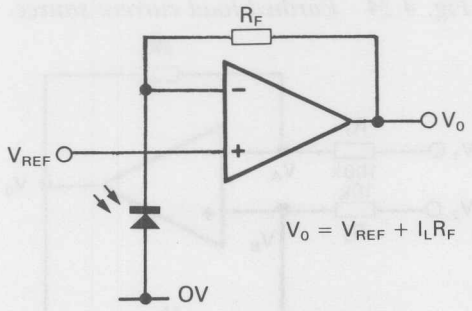
For single input control put V_1 input to ground.

Basic Photo Diode Receiver

The basic circuit is shown in Figure 4.25. The non-inverting input is held at V_{ref}, and the feedback resistor R_F causes a virtual earth at the

inverting input. This defines the reverse bias across the photo diode. The very low input bias currents of the LinCMOS op-amps do not mask the dark current of the photo diode as can occur with bipolar op-amps. Thus the circuit can be used for detecting low light intensities.

Fig. 4.25 Basic photo diode receiver.



COMPOSITE LOW DRIFT AMPLIFIERS

Fast Low Drift Amplifier Using TLC271 and LM318

Op-amps in composite connections are cost effective solutions where amplifiers with both high slew rate and good offset voltage specifications are required. Figure 4.26 shows the TLC271 with its low off-set drift teamed with the LM318's 50V/μs slew rate. The TLC271 is used, where it has best drift performance, in low bias mode. Typical instrumentation applications are in fast rectifiers and logarithmic converters.

At d.c., using the large loop gain of the TLC271, the output voltage drift is equal to the TLC271 input offset drift multiplied by the non-inverting gain of the LM318. The offset voltage of the LM318 is continuously nulled by forcing the summing node to equal the offset of the TLC271. This is achieved by the use of a secondary feedback loop formed by R_1, R_2 and the LM318's input stage.

Fig. 4.26 Fast low drift amplifier.

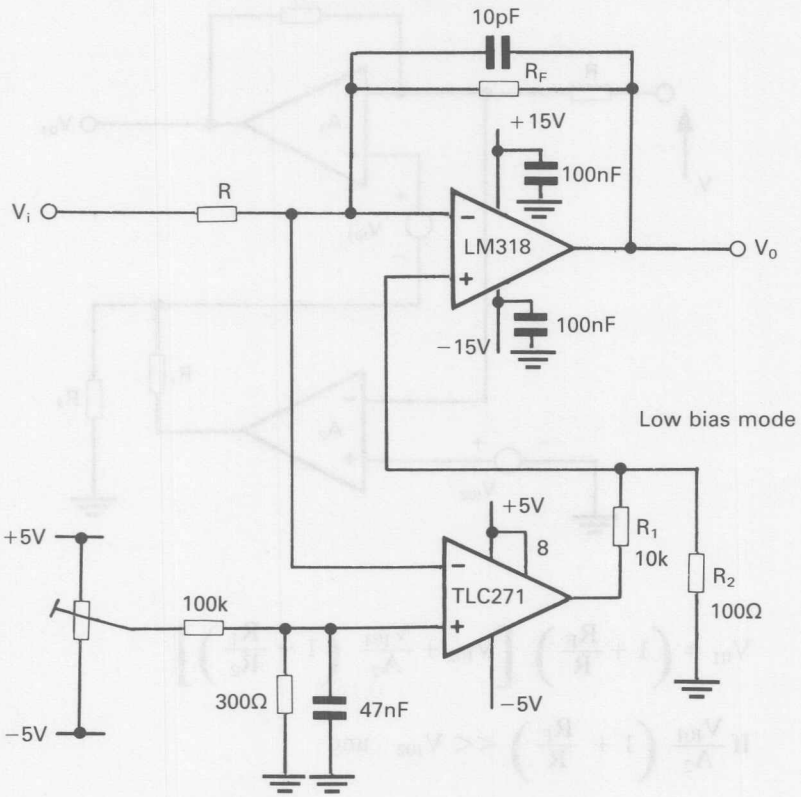
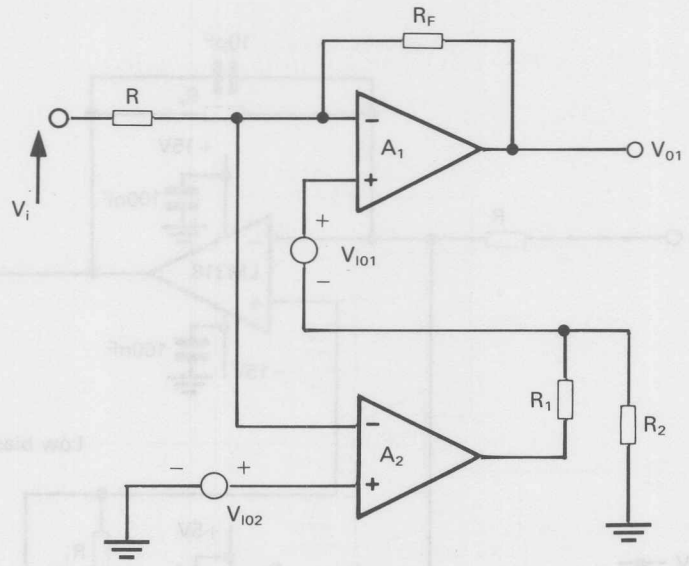


Figure 4.27 shows the d.c. feedback loop analysed for offset voltage drift as follows assuming $V_i = 0$:

$$V_{01} = \left[-V_{01} \frac{R}{R + R_F} + \left(-V_{01} \frac{R}{R + R_F} + V_{I02} \right) A_2 \frac{R_2}{R_1 + R_2} + V_{I01} \right] \times A_1$$

Rearranging with assumptions that: $\frac{1}{A_1} << 1$ & $A_2 \frac{R_2}{R_1 + R_2} >> 1$

Fig. 4.27 Fast low drift amplifier D.C. analysis.



$$V_{01} = \left(1 + \frac{R_F}{R}\right)\left[V_{I02} + \frac{V_{I01}}{A_2}\left(1 + \frac{R_1}{R_2}\right)\right]$$

$$\text{If } \frac{V_{I01}}{A_2}\left(1 + \frac{R_F}{R}\right) << V_{I02} \quad \text{and}$$

$$\frac{dV_{I01}/dT}{A_2}\left(1 + \frac{R_1}{R_2}\right) << dV_{I02}/dt$$

$$\text{Then: } V_{01} = \left(1 + \frac{R_F}{R}\right)V_{I02}; \qquad \frac{dV_{01}}{dT} = \left(1 + \frac{R_F}{R}\right)\frac{dV_{I02}}{dT}$$

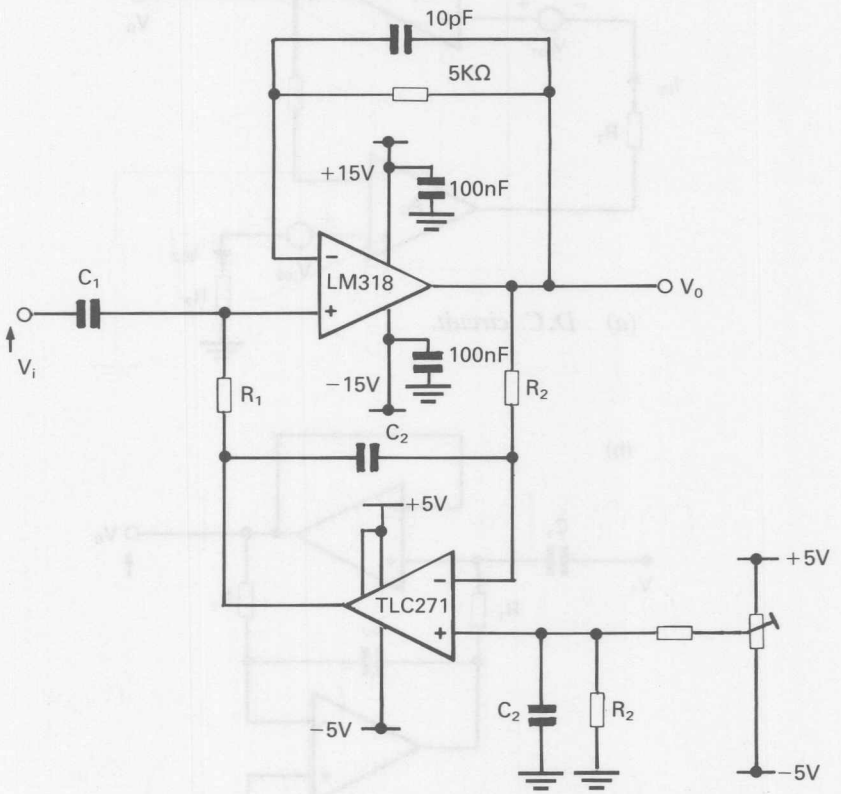
The error due to bias current drift is dominated by the LM318 where $V_{01} = R_F.I_{IB}$ (LM318) $\therefore$ $dV_{01}/dT = R_F \cdot dI_{IB}/dT$ and limits the practical values of feedback resistors to a few kohms.

Fast Low Drift AC. Buffer using TLC271 and LM318

A composite connection has advantages in applications where a fast a.c. buffer is required and d.c. output error voltage cannot be tolerated.

Examples of such circuits are sample and hold and A/D converters. A composite circuit using a TLC271 and LM318 is shown in Figure 4.28.

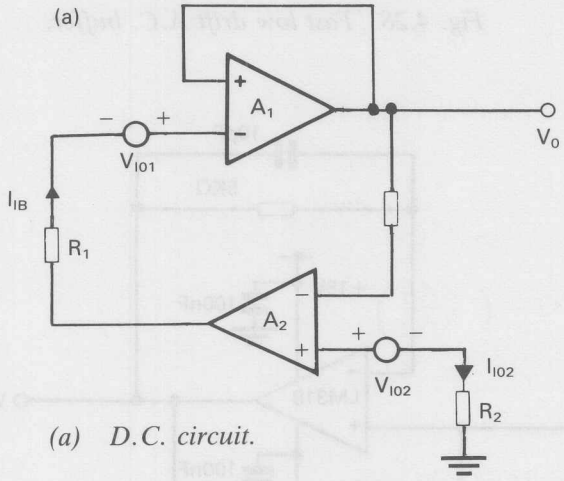
Fig. 4.28 Fast low drift A.C. buffer.



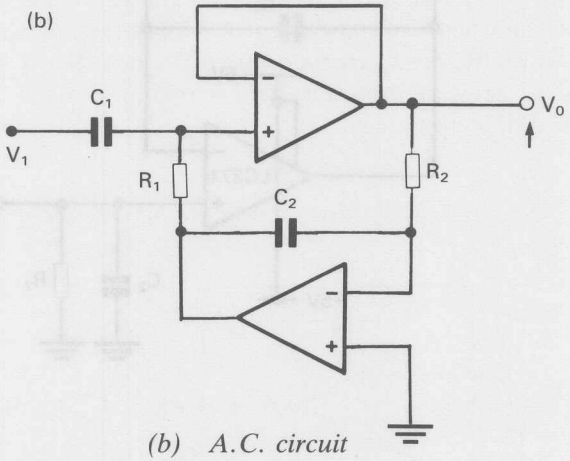
The output voltage V_0 is integrated by R_2C_2 and compared to zero volts by TLC271. The difference, integrated again by R_1C_1, adjusts the input d.c. level of the LM318 noninverter connected amplifier to give zero d.c. output voltage. A reasonable choice of R_2 will give an output offset drift equal to the TLC271 specification. The zeroing circuit forms an active second order highpass filter from V_i to V_o.

Figure 4.29 (a) & (b) show the d.c. and a.c. circuits respectively.

Fig. 4.29



(a) D.C. circuit.



(b) A.C. circuit

The d.c. conditions of Figure 4.29(a) are analysed assuming R_{in} of $A_2 >> R_2$ equating voltages at node A:

$$V_0 - V_{I01} + I_{IB}R_1 = (-V_0 + V_{I02} + I_{I02}R_2)A_2$$

If A_2 tends to infinity then:

$$V_0 = V_{I02} + I_{I02}R_2 \quad \& \quad \frac{dV_0}{dT} = \frac{dV_{I02}}{dT} + R_2\frac{dI_{I02}}{dT}$$

The a.c. analysis of Figure 4.29(b) yields:

$$\frac{V_0}{Vi} = \frac{s^2}{s^2 + (1/R_1C_1)s + (1/R_1R_2C_1C_2)} = \frac{s^2}{s^2 + s(\omega_O/Q) + {\omega_O}^2}$$

$$\text{then: } Q = \left(\frac{R_1C_1}{R_2C_2}\right)^{1/2} \quad \& \quad \omega_o = (R_1R_2C_1C_2)^{-1/2}$$

Choose C_1 and C_2; then $R_1 = Q/C_1\omega_o$ & $R_2 = 1/C_2Q.\omega_o$

VOLTAGE REGULATORS

Figure 4.30 shows a low quiescent power voltage regulator that consumes only 60μA of standby current using the low bias mode. A load regulation of 10% can achieved for the values shown. Capacitor C_c is included to prevent instability which manifests itself by higher than expected quiescent current.

Fig. 4.30 Low power voltage regulator.

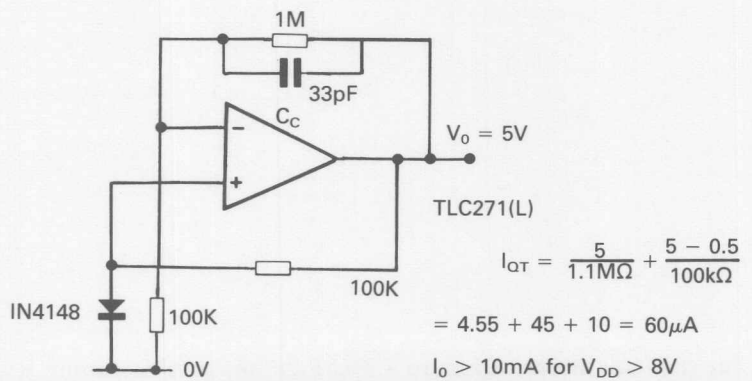
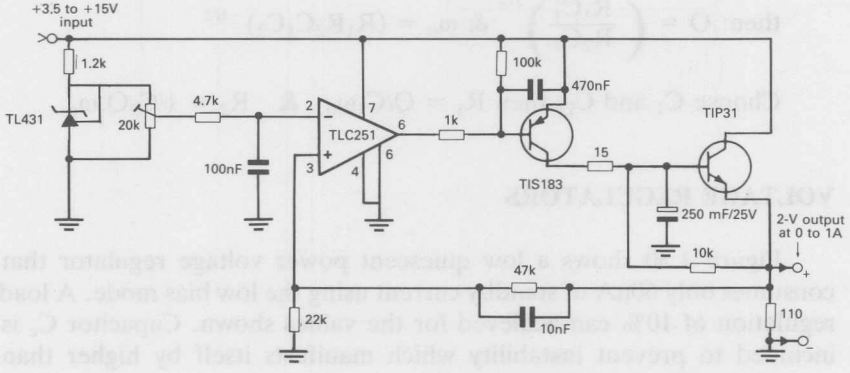


Figure 4.31 shows a low voltage regulator circuit employing a TLC251 1V op-amp. There is seldom need to design a new regulator with the variety of monolithic regulators now available. However many new devices, such as gate arrays and logic circuits, require a regulated voltage as low as 2–3 volts. Gate arrays require a well regulated supply of 2 volts at typical current of 250mA. With several of these devices in a system a current of 1A may be needed from a wide input voltage range, particularly 5V or less. In such applications the TLC251 can provide the loop gain needed to give a regulation of ±20mV over the 1A load range.

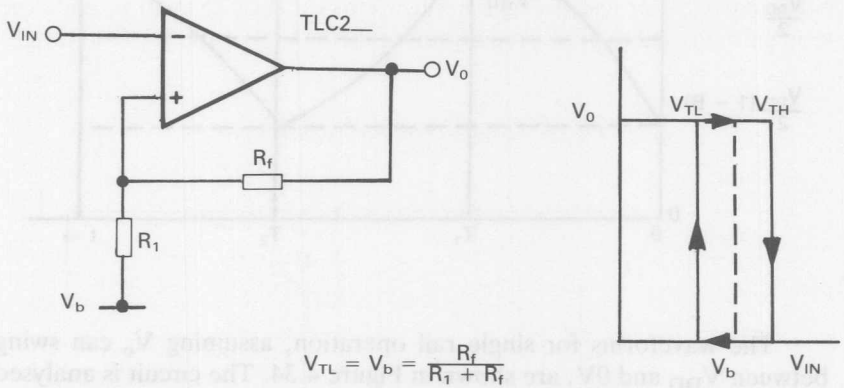
Fig. 4.31 2V voltage regulator.



BASIC SCHMITT TRIGGER

An example is shown in Figure 4.32 for single rail operation centred on V_b. For symmetrical operation V_b should be $V_{OM}/2$.

Fig. 4.32 Basic Schmitt trigger.



$$V_{TL} = V_b = \frac{R_f}{R_1 + R_f}$$

$$V_{TH} = V_b \frac{R_f}{R_1 + R_f} + \frac{V_{OM}\, R_1}{R_1 + R_f}$$

OSCILLATOR CIRCUITS

Astable Squarewave

Adding a RC network to a Schmitt trigger forms the classic op-amp astable op-amp astable circuit. (Figure 4.33).

Fig. 4.33 Astable oscillator.

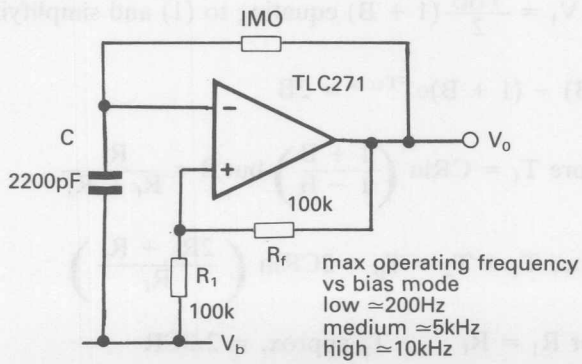
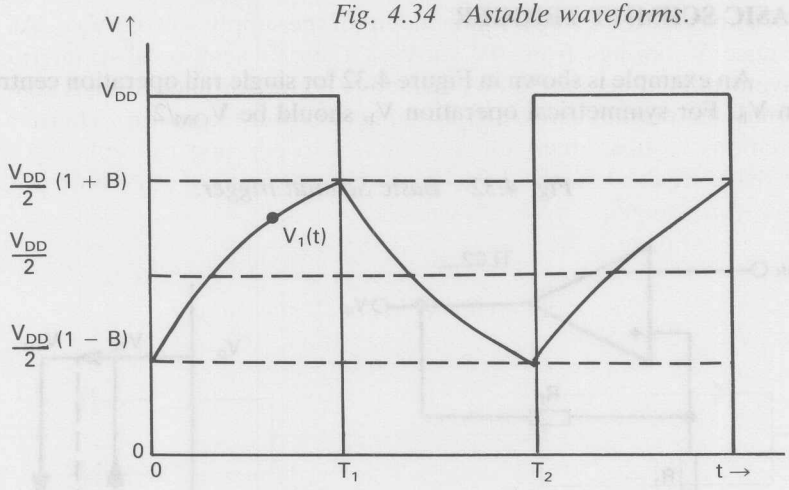


Fig. 4.34 Astable waveforms.



The waveforms for single rail operation, assuming V_o can swing between V_{DD} and 0V, are shown in Figure 4.34. The circuit is analysed as follows:

V_1 as a function of time $V_1(t)$ is given by:

$$V_1(t) = \left(V_{DD} - \frac{V_{DD}}{2}(1 - B)\right)(1 - e^{-t/CR}) + \frac{V_{DD}}{2}(1 - B) \quad (1)$$

at T_1; $V_1 = \frac{V_{DD}}{2}(1 + B)$ equating to (1) and simplifying.

$$(1 + B) - (1 + B)e^{-T_{1/C.R}} = 2B$$

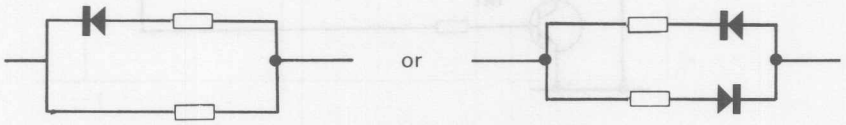
$$\text{therefore } T_1 = CR\ln\left(\frac{1 + B}{1 - B}\right) \text{ but } B = \frac{R_1}{R_f + R_1}$$

$$\text{therefore } T_1 + T_2 = T_p = 2CR\ln\left(\frac{2R_1 + R_f}{R_f}\right)$$

and for $R_1 = R_f$ $\quad T_p$ approx. $= 2.2CR$

Thus the frequency is independent of the supply voltage V_{DD}. As in practice V_o swings from 0V to V_{OM} then to achieve a symmetrical waveform the bias should be adjusted to $V_{OM}/2$ or back to back zeners should be placed across R_f to limit the output swing. There are variations to this circuit for asymmetrical operation by replacing the feedback resistor with diode/resistor combinations to control the capacitor changing rate as shown in Figure 4.35.

Fig. 4.35 Astable feedback alternatives.



The low input bias currents of the LinCMOS op-amps allow high values of resistor and lower non-electrolytic values of capacitor for high accuracy and wide mark-space ratios. Minimum pulse widths achievable will be determined by op-amp slew rate performance and hence for the smallest pulses high bias mode should be used.

Single Rail VCO

A voltage controlled oscillator that operates on a single rail is shown in Figure 4.36.

Op-amp A_1 operates as an integrator with an input voltage $\pm V_{in}/2$ set by voltage divider R_1 and R_2, integrating from $+V_{in}/2$ when TR1 is off and $-V_{in}/2$ when TR1 is on. By making $R_4 = \frac{1}{2}R_3$ integrating currents are equal for each period. Figure 4.37 shows the waveforms and the frequency of oscillation is derived as follows:

$$\text{During time } T_1; \quad V_1(t) = -\frac{V_{in}}{2CR}t + \frac{V_{DD}}{2}(1 + B)$$

$$\text{at } T_1; \quad V_1 = \frac{V_{DD}}{2}(1 - B)$$

Fig. 4.36 Voltage controlled oscillator.

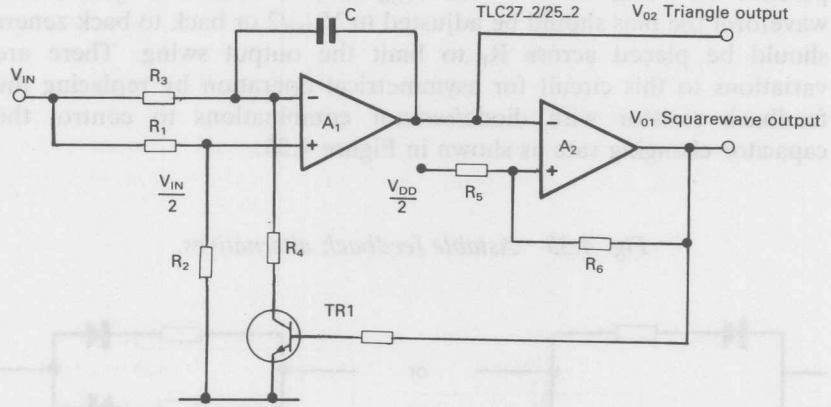
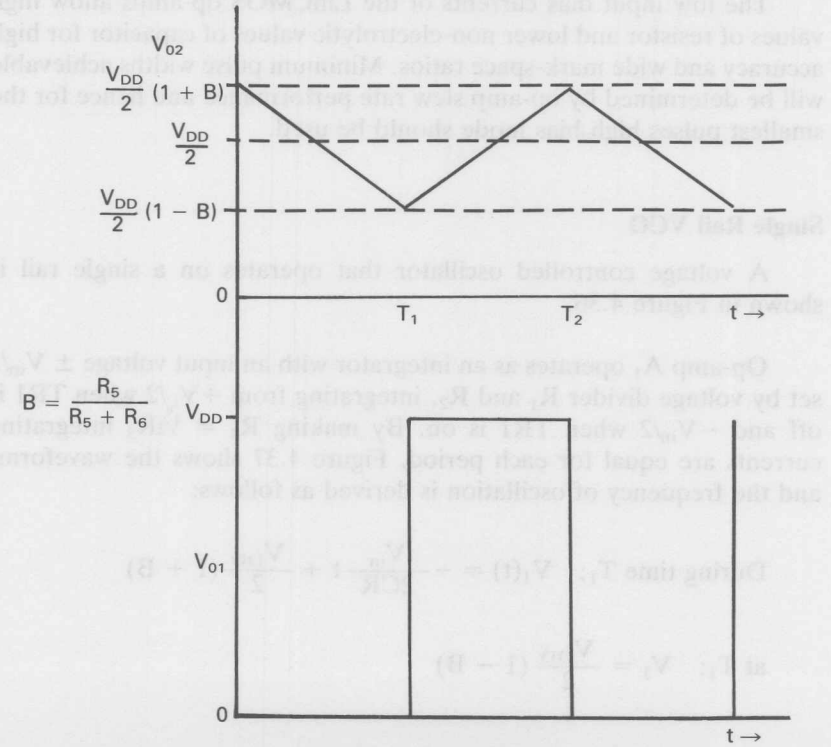


Fig. 4.37 Waveforms.

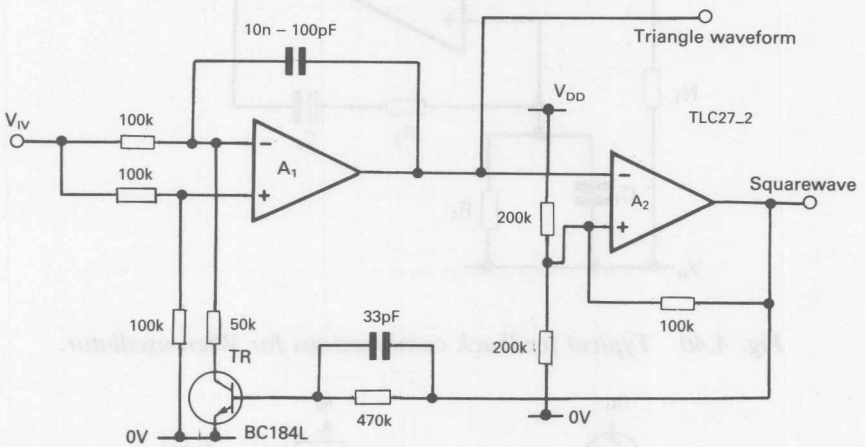


$$\text{therefore } \frac{V_{DD}}{2}(1 - B) = -\frac{V_{in}T_1}{2CR} + \frac{V_{DD}}{2}(1 + B)$$

$$\text{therefore } T_1 = \frac{2CRV_{DD}.B}{V_{in}} \quad \text{or} \quad f_{osc} = \frac{V_{in}(R_5 + R_6)}{4CRV_{DD}R_5}$$

Thus the frequency of operation is proportional to input voltage V_{in}. See Figure 4.38 for a circuit with some typical component values.

Fig. 4.38 VCO with typical values.



base low bias 200Hz
medium bias 5KHz
high bias 30KHz
} Slew rate limited

Asymmetry is due to TR switching times.

Wien Bridge Sinewave Oscillator

The classic low distortion sine wave oscillator is shown in Figure 4.39.

Fig. 4.39 Wien bridge oscillator.

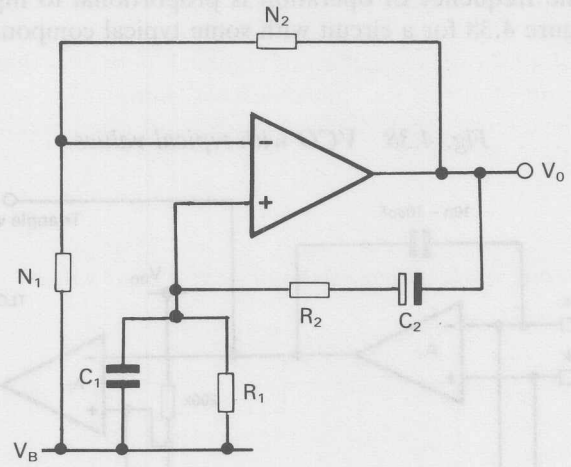
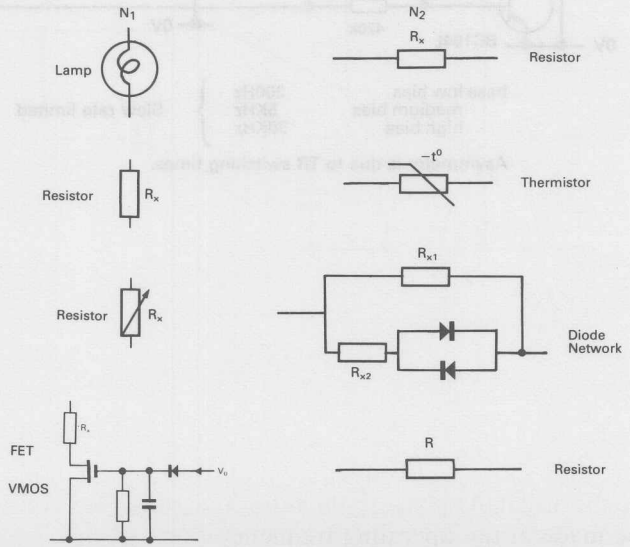


Fig. 4.40 Typical feedback combinations for Wien oscillator.



This has a frequency of oscillation $f_o = 1/[2\pi\sqrt{R_1R_2C_1C_2}] = 1/(2\pi RC)$ for equal component values. The attenuation of this feedback circuit at zero phase shift is 1/3 and thus the amplifier must provide a gain of exactly 3 to sustain oscillations. This is achieved by automatic amplitude control which provides an amount of negative feedback dependent on the output amplitude. Thus the circuit will oscillate at any output amplitude that satisfies the gain of 3 requirement.

Figure 4.40 shows a selection of feedback networks that have been used for gain control i.e. incandescent lamp (+ve temp coef), thermistor −ve temp coef), diode networks and n-channel junction and VMOS FETs.

Fig. 4.41 Wien oscillator with typical values.

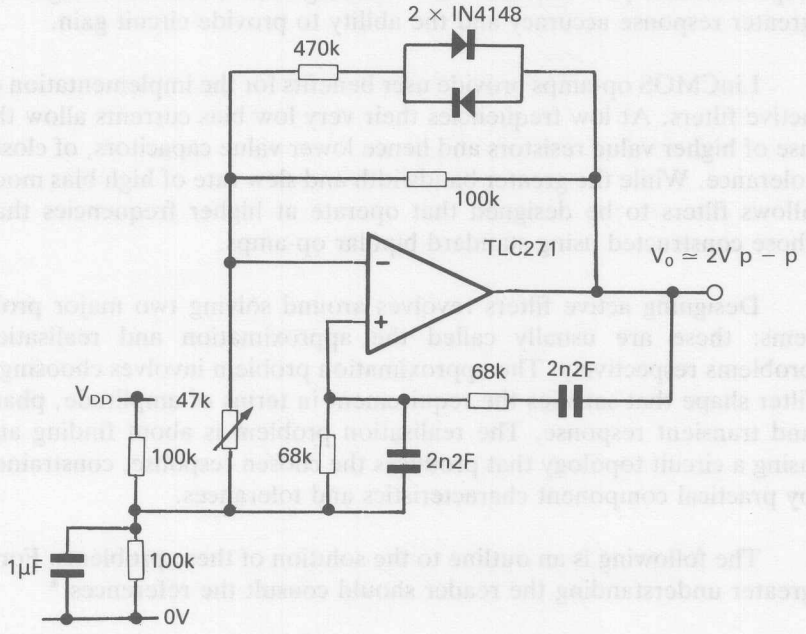


Figure 4.41 shows a circuit with typical values for a diode feedback network, the usual A_{OL}/A_{CL} gain ratio and slew rate considerations should be made at the operating frequency.

ACTIVE FILTERS

Introduction

Active filters employ op-amps with passive resistive and capacitive components to synthesise filters with the characteristics of lumped R-L-C circuits. Essentially this allows the resonance effects of R-L-C circuits to be reproduced by passive and active components using energy from the power supply. This can be understood in terms the pole-zero diagram where the poles of passive R-C networks, that lie on the negative real axis, are moved into the complex plane to form conjugate pairs. Thus the desirable characteristics of R-L-C networks are achieved.

Active filters have many advantages over their R-L-C counterparts especially at low frequencies where the elimination of large inductors improves filter performance while reducing cost. Other advantages are greater response accuracy and the ability to provide circuit gain.

LinCMOS op-amps provide user benefits for the implementation of active filters. At low frequencies their very low bias currents allow the use of higher value resistors and hence lower value capacitors, of closer tolerance. While the greater bandwidth and slew rate of high bias mode allows filters to be designed that operate at higher frequencies than those constructed using standard bipolar op-amps.

Designing active filters revolves around solving two major problems: these are usually called the approximation and realisation problems respectively. The approximation problem involves choosing a filter shape that satisfies the requirement in terms of amplitude, phase and transient response. The realisation problem is about finding and using a circuit topology that produces the chosen response, constrained by practical component characteristics and tolerances.

The following is an outline to the solution of these problems. For a greater understanding the reader should consult the references.*

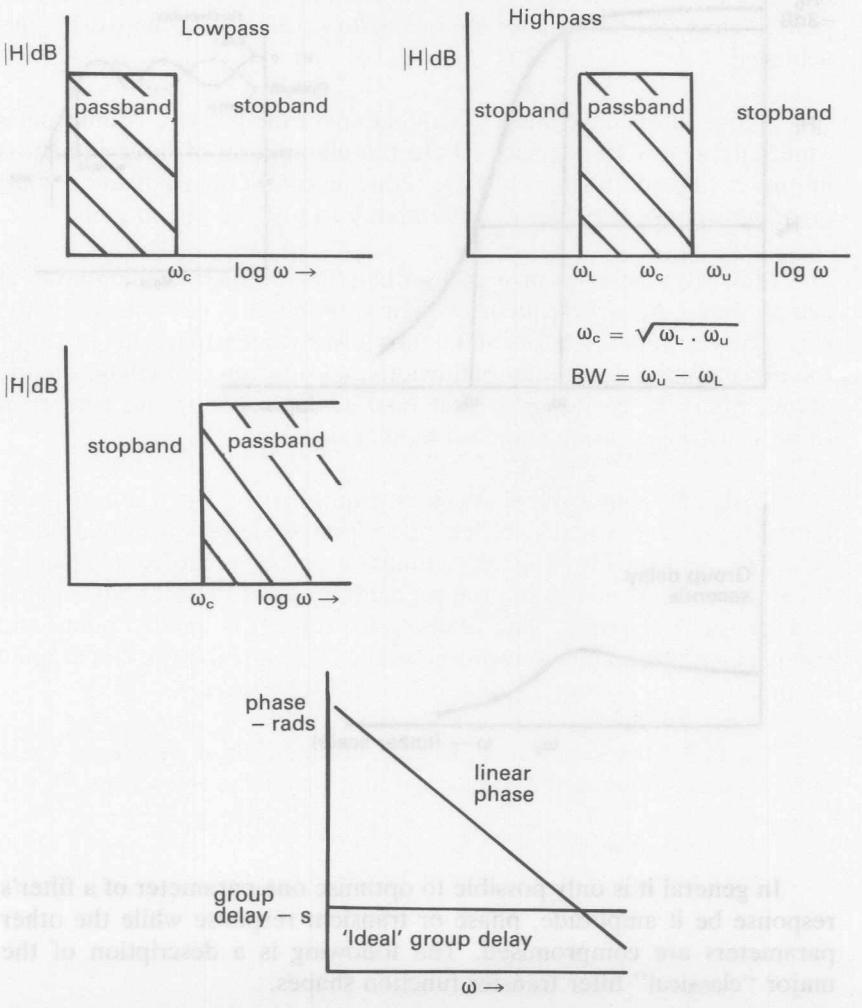
*see references 2 to 7

Approximation Problem

Ideal Response

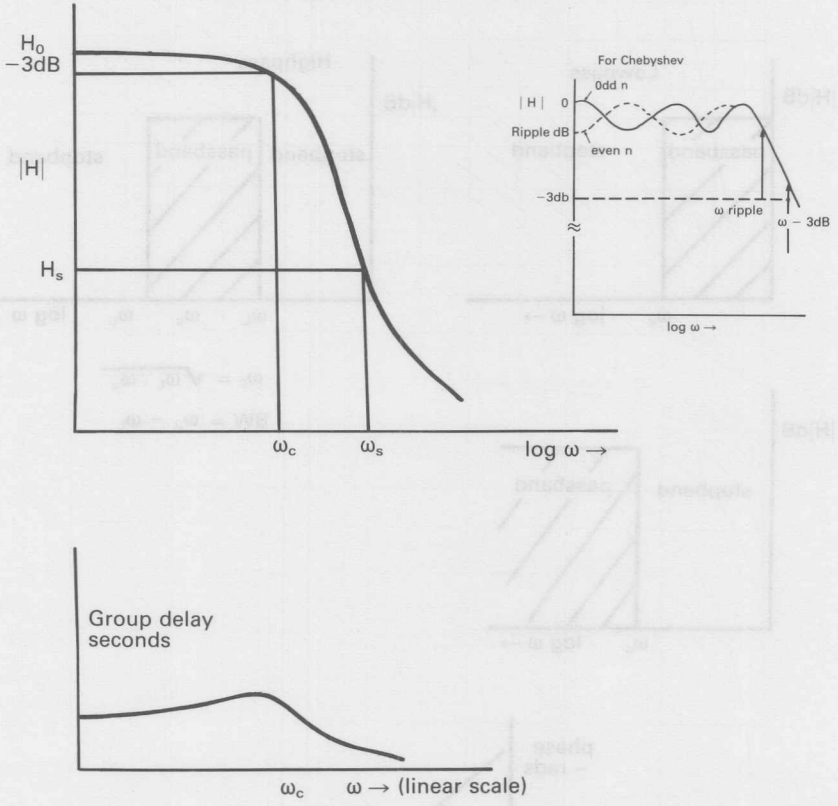
The ideal "brickwall" filter is represented by constant amplitude and group delay (linear phase) in the passband and zero transmission in the stopband (Figure 4.42).

Fig. 4.42 Ideal 'Brickwall' filter responses.



Practical filters have amplitude deviations in the passband, varying amounts of slope in the transition from passband to stopband and finite stopband transmission. Group delay (phase response), unless specifically optimised, will be non-linear particularly at the band edges. (Figure 4.43).

Fig. 4.43 Practical filter responses.



In general it is only possible to optimise one parameter of a filter's response be it amplitude, phase or transient response while the other parameters are compromised. The following is a description of the major "classical" filter transfer function shapes.

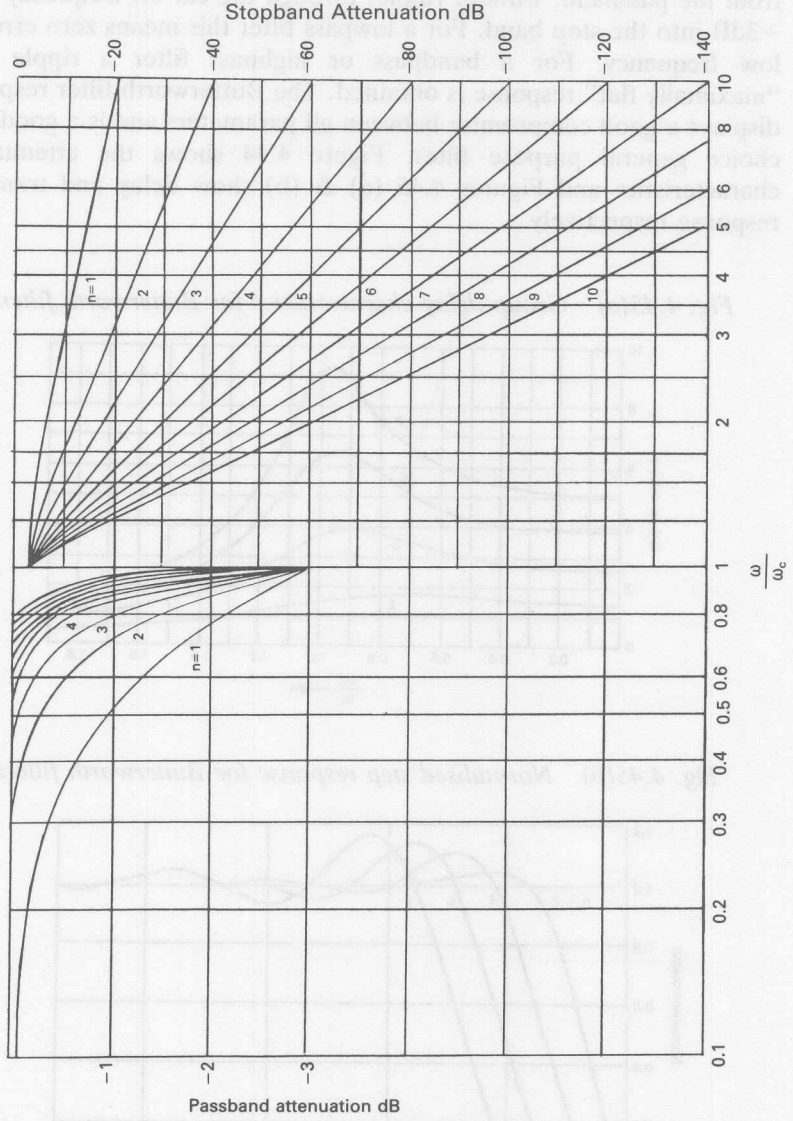


Fig. 4.44 Butterworth attenuation characteristic.

Butterworth-Maximally Flat Amplitude

The Butterworth shape is "maximally flat" and proceeds smoothly from the passband, without ripple, through the cut-off frequency f_c at −3dB into the stop band. For a lowpass filter this means zero error at low frequency. For a bandpass or highpass filter a ripple free "maximally flat" response is obtained. The Butterworth filter response displays a good compromise between all parameters and is a good first choice general purpose filter. Figure 4.44 shows the attenuation characteristics and Figures 4.45 (a) & (b) show delay and transient response respectively.

Fig. 4.45(a) Group-delay characteristics for Butterworth filters.

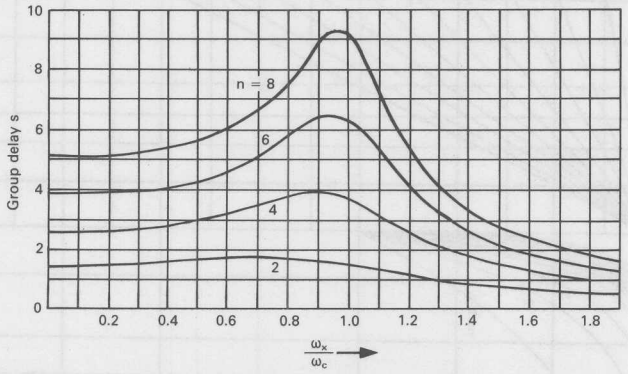
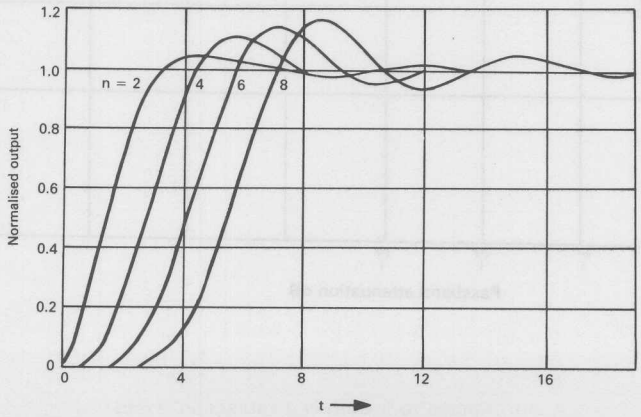


Fig. 4.45(b) Normalised step response for Butterworth filters.



The amplitude response H of a Butterworth filter is given by:

$$|H(j\omega)| = \frac{H_o}{[1 + (\omega/\omega_c)^{2n}]^{1/2}}$$

Normalised attenuation $A = [1 + (\omega/\omega_c)^{2n}]^{1/2}$.

Rearranging this, the order of filter n can be determined for slope factor ω_s/ω_c at attenuation $H_s = A$

$$n \geq \frac{\log (A^2 - 1)}{2\log (\omega_s/\omega_c)}$$

$$\text{For A in dB's } n \geq \frac{\log (10^{Adb/10} - 1)}{2\log (\omega_s/\omega_c)}$$

where ω_c is −3dB filter bandwidth in rads-sec.

The attenuation rate beyond cut-off ω_c is n × −20dB/decade. The pole positions for the Butterworth filter are given in Table 4.2(a).

Table 4.2 Butterworth & Bessel pole locations.

	(a) Butterworth Pole Locations		(b) Bessel Pole Locations	
Order *n*	Real Part $-\alpha$	Imaginary Part $\pm j\beta$	Real Part $-\alpha$	Imaginary Part $\pm j\beta$
2	0.7071	0.7071	1.1030	0.6368
3	0.5000 1.0000	0.8660	1.0509 1.3270	1.0025
4	0.9239 0.3827	0.3827 0.9239	1.3596 0.9877	0.4071 1.2476
5	0.8090 0.3090 1.0000	0.5878 0.9511	1.3851 0.9606 1.5069	0.7201 1.4756
6	0.9659 0.7071 0.2588	0.2588 0.7071 0.9659	1.5735 1.3836 0.9318	0.3213 0.9727 1.6640
7	0.9010 0.6235 0.2225 1.0000	0.4339 0.7818 0.9749	1.6130 1.3797 0.9104 1.6853	0.5896 1.1923 1.8375
8	0.9808 0.8315 0.5556 0.1951	0.1951 0.5556 0.8315 0.9808	1.7627 0.8955 1.3780 1.6419	0.2737 2.0044 1.3926 0.8253

normalised to 1 ohm & 1 rad/sec at −3dB

Chebyshev Equiripple Passband

Chebyshev transfer function shapes show greater selectivity close to the cut-off frequency than either Butterworth or Bessel (see below) at the expense of ripple in the passband. Chebyshev filters can be designed with passband ripples from 0.01 to 3dB but the range 0.1 to 1dB is most useful. Bandwidths (ω_c) are quoted at either the equiripple point entering the stopband or at the −3dB point. This is an item to watch out for, when using filter tables from different sources, to prevent inaccuracies in the final filter design. The tables of lowpass pole positions given here are normalised to 1 ohm and 1 rad/second at the −3dB point.

Figure 4.46 and 4.47 show the group delay and transient response respectively of Chebyshev 0.5dB ripple filters and these are clearly worse than those for Butterworth or Bessel (see below).

Fig. 4.46 Group-delay characteristics for Chebyshev filters with 0.5–dB ripple.

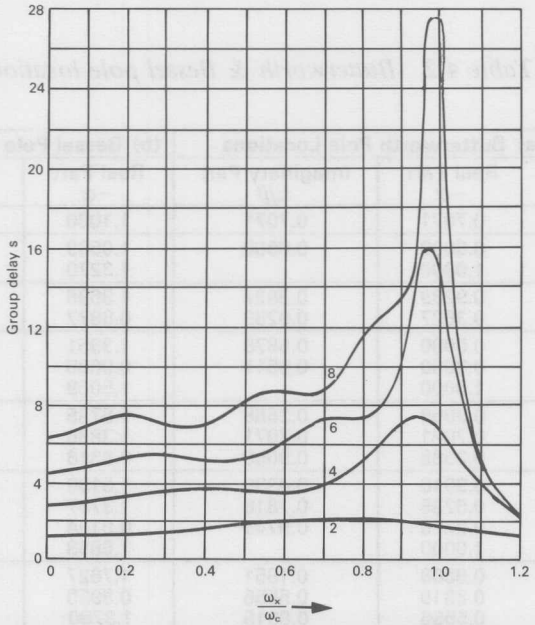
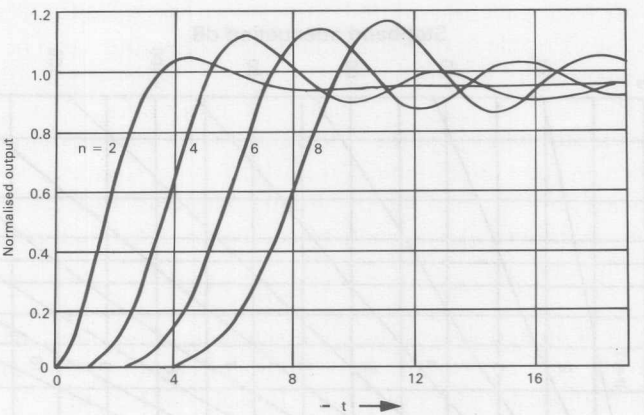


Fig. 4.47 Step response for Chebyshev filters with 0.5–dB ripple.



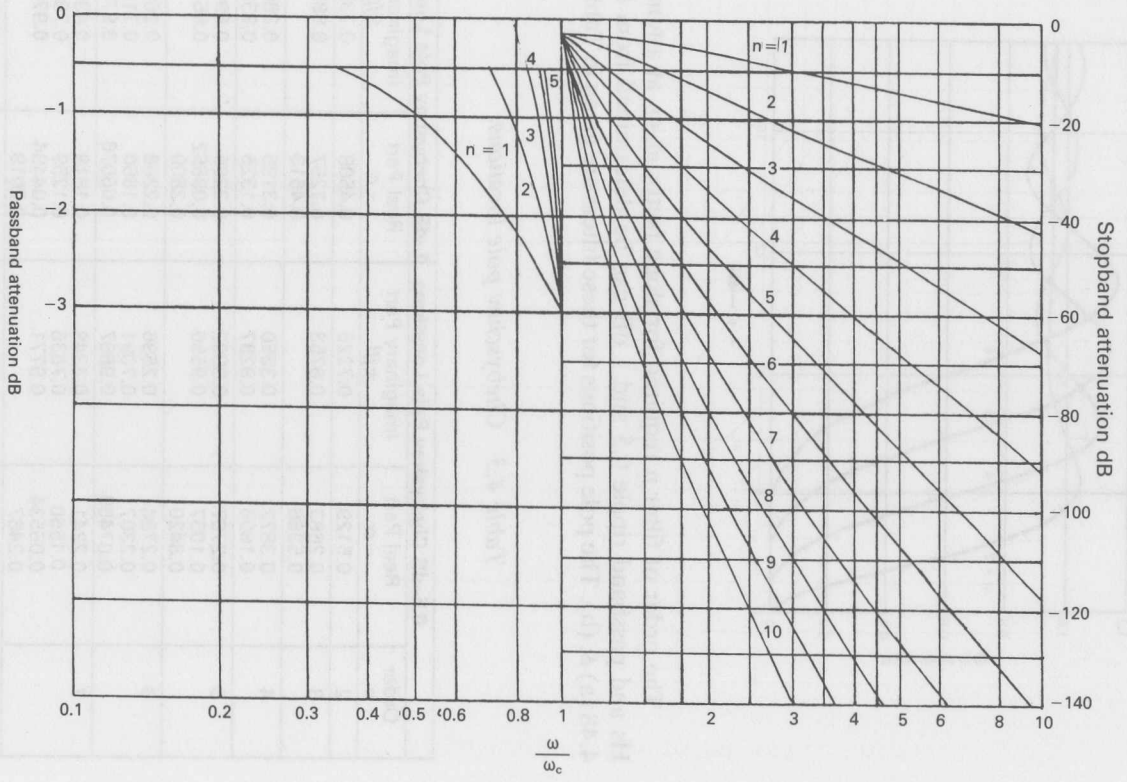
The order of filter n required for slope factor ω_s/ω_c at attenuation Hs and passband ripple 0.5 and 1 dB can be determined from Figure 4.48 (a) & (b). The pole positions for these filters are given in Table 4.3.

Table 4.3 Chebyschev pole locations.

	0.5–dB Chebyshev Pole Locations		1–dB Chebyshev Pole Locations	
Order *n*	Real Part $-\alpha$	Imaginary Part $\pm j\beta$	Real Part $-\alpha$	Imaginary Part $\pm j\beta$
2	0.5129	0.7225	0.4508	0.7351
3	0.2683 0.5366	0.8753	0.2257 0.4513	0.8822
4	0.3872 0.1605	0.3850 0.9297	0.3199 0.1325	0.3868 0.9339
5	0.2767 0.1057 0.3420	0.5902 0.9550	0.2265 0.08652 0.2800	0.5918 0.9575
6	0.2784 0.2307 0.07459	0.2596 0.7091 0.9687	0.2268 0.1660 0.06076	0.2601 0.7106 0.9707
7	0.2241 0.1550 0.05534 0.2487	0.4349 0.7836 0.9771	0.1819 0.1259 0.04494 0.2019	0.4354 0.7846 0.9785
8	0.2144 0.1817 0.1214 0.04264	0.1955 0.5565 0.8328 0.9824	0.1737 0.1473 0.09840 0.03456	0.1956 0.5571 0.8337 0.9836

normalised to 1 ohm & 1 rad/sec at −3dB

Fig. 4.48(a) Chebyshev attenuation characteristic with 0.5dB ripple.



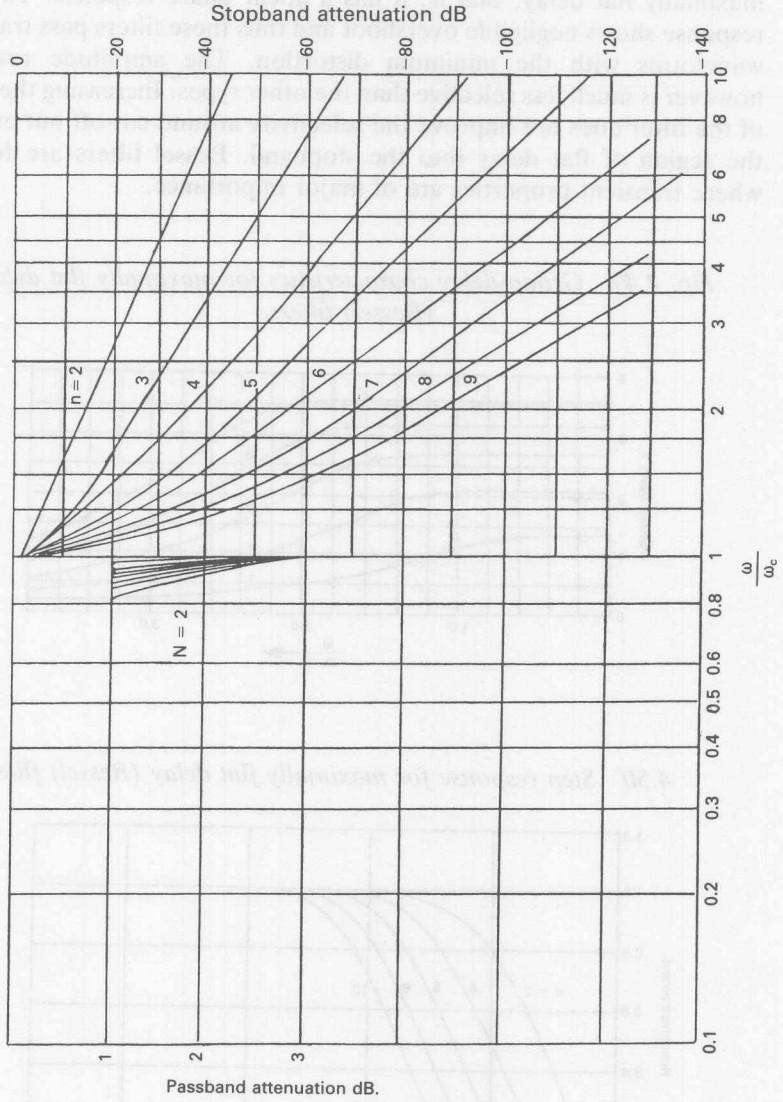
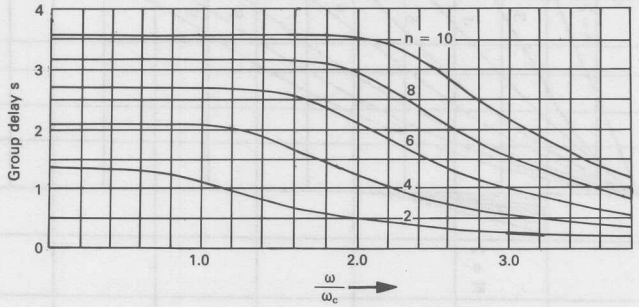


Fig. 4.48(b) Chebyshev attenuation characteristic with 1dB ripple.

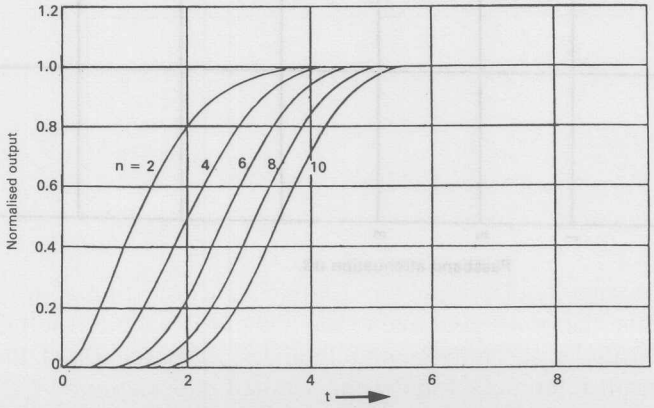
Bessel-Maximally Flat Delay

The Bessel transfer function has been optimised to obtain a maximally flat delay; that is, it has a linear phase response. The step response shows negligible overshoot and thus these filters pass transient waveforms with the minimum distortion. The amplitude response however is much less selective than the other types. Increasing the order of the filter does not improve the selectivity around cut-off but extends the region of flat delay into the stopband. Bessel filters are for use where transient properties are of major importance.

Fig. 4.49 Group-delay characteristics for maximally flat delay (Bessel) filters.



4.50 Step response for maximally flat delay (Bessel) filters.

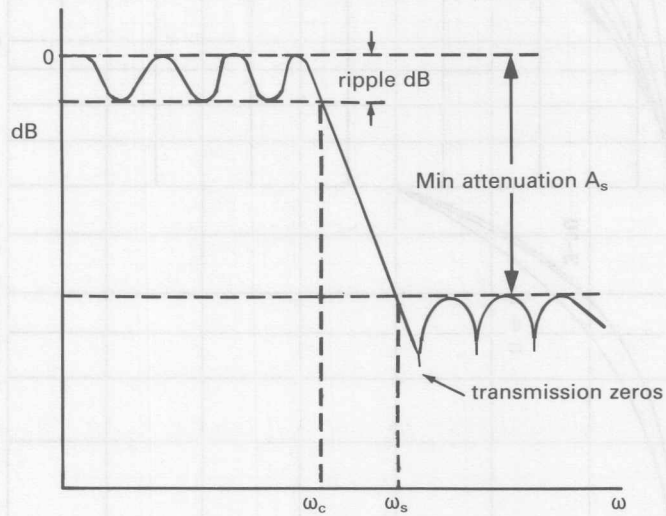


Figures 4.49 and 4.50 give the group delay and transient responses respectively. The order of filter required for shape factor ω_s/ω_c at attenuation Hs can be determined from Figure 4.51 and the pole positions are given in Table 4.2(b).

Elliptic (Cauer)-Function

Elliptic function filters feature stopband transmission zeros and have the sharpest roll-off characteristics for a given number of poles. Improved roll-off performance is obtained at the expense of return lobes in the stopband Figure 4.52.

Fig. 4.52 Typical elliptic-function low-pass filter response.



The circuit realizations for Elliptic function filters are more complex than the others and due to the higher Q's required suffer from greater sensitivity to component tolerances. It is suggested that the reader consult references 4 and 5 for detailed information.

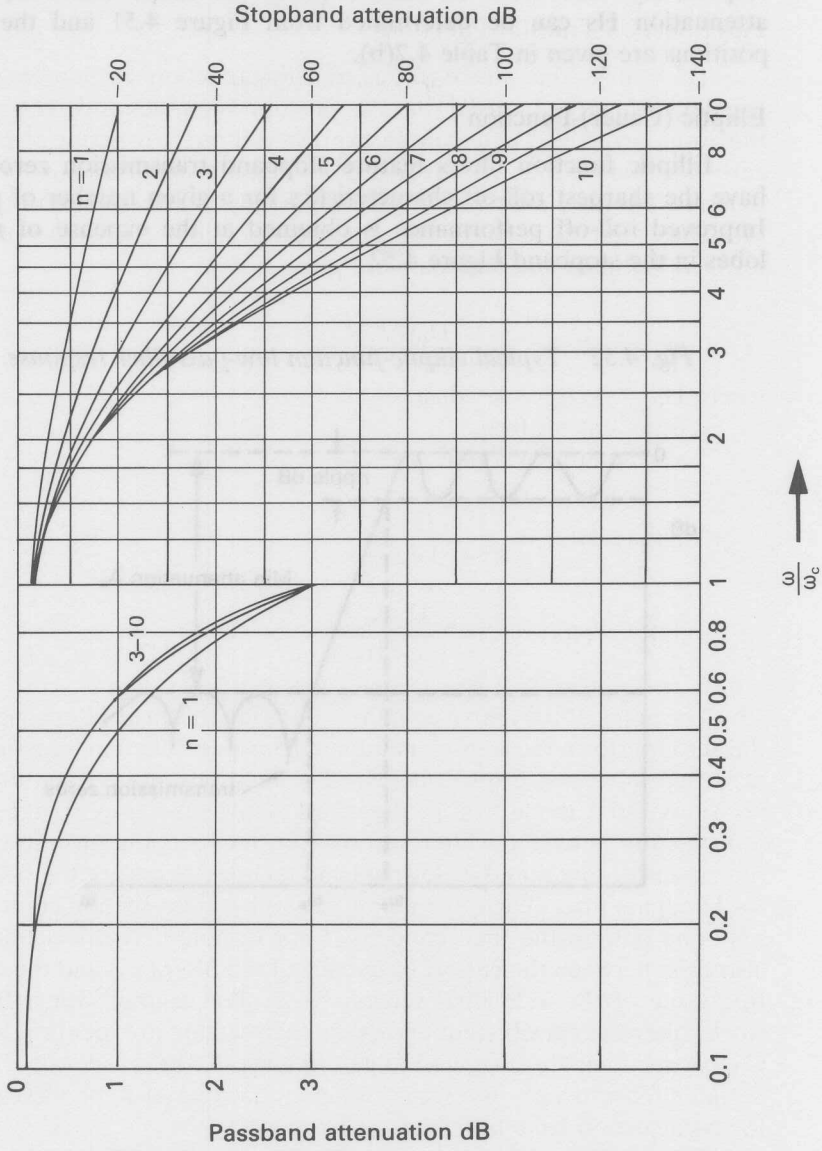


Fig. 4.51 Bessel attenuation characteristic.

Realisation of Filter Transfer Functions

Filter Section Transfer Functions

To realise the above filter transfer function responses circuit topologies have to be used that can position the poles and zeros of the function correctly. These can be expressed directly in terms of pole or zero positions $-\alpha \pm j\beta$ but are more usually expressed in terms of damping d (or it's inverse Q = 1/d for bandpass) and resonant frequency ω_o. The standard network transfer functions for a two pole (n = 2) lowpass highpass and bandpass are given below:

$$\text{Lowpass } H(s) = \frac{H_o\omega_o^2}{s^2 + d\omega_o s + \omega_o^2}$$

where H_o = Amplitude const.
ω_o = cut-off freq.
s = complex variable.

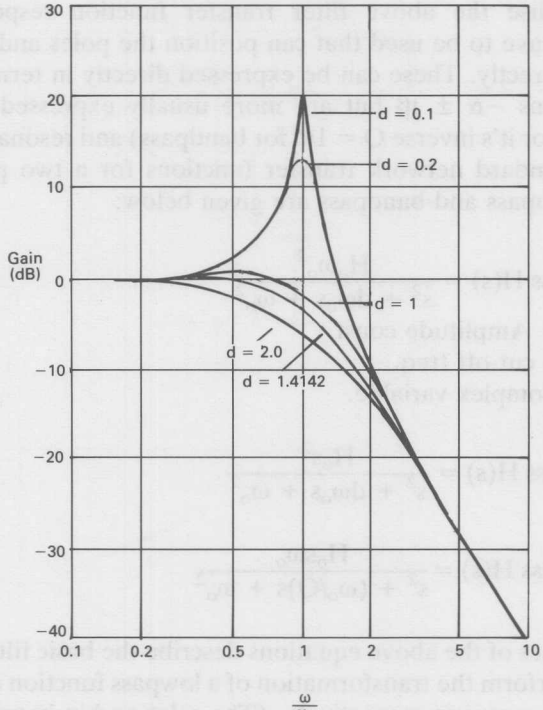
$$\text{Highpass } H(s) = \frac{H_o s^2}{s^2 + d\omega_o s + \omega_o^2}$$

$$\text{Bandpass } H(s) = \frac{H_o s\omega_o}{s^2 + (\omega_o/Q)s + \omega_o^2}$$

The poles of the above equations describe the basic filter shape and the zeros perform the transformation of a lowpass function into highpass or bandpass response respectively. (The relationship between the pole positions and d and ω_o will be described below.) It is important to draw a distinction between a filter section transfer function and the overall filter transfer function. For lowpass and highpass these are the same but for bandpass filters each two pole (2nd order) filter section contributes only one pole to the final bandpass filter response. A distinction may also exist between the cut-off frequency of the filter (ω_c) and the cut-off frequency of the individual sections (ω_o). For example for a Butterworth filter the cut-off frequencies for each section are identical but for Chebyshev they are staggered to get the overall filter response. Thus to design a filter to a given response shape the values of d (or 1/Q) and ω_o for each section have to be set.

Figure 4.53 shows how the amplitude response of a lowpass two pole section varies with change of damping d. Frequency ω_o is adjusted to position this amplitude response.

Fig. 4.53 Normalised amplitude response Vs. damping d for 2nd order lowpass filter.



In summary an overall filter response shape is manipulated by the adjustment of the individual 2nd order filter sections damping d and resonant frequency ω_o.

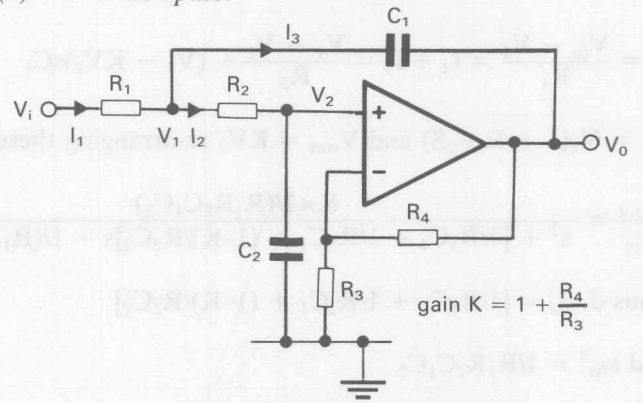
Filter Circuit Topologies

Voltage Controlled Voltage Source (VCVS)

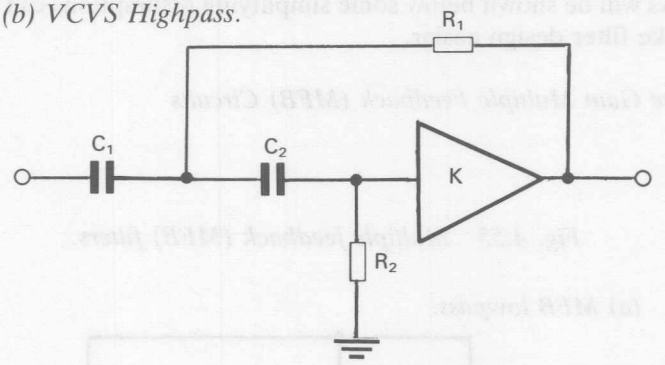
Otherwise known as Sallen and Key circuits these use a positive gain K and as shown by Figure 4.54 can be used to implement all types of filters.

Fig. 4.54

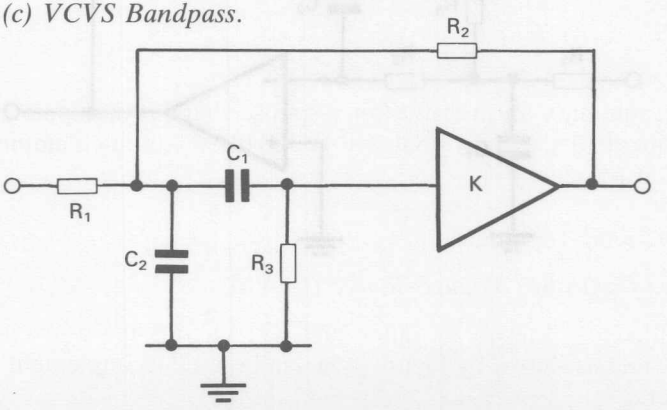
(a) VCVS Lowpass.



(b) VCVS Highpass.



(c) VCVS Bandpass.



They are most successful with low and highpass filters of damping > 0.5. An example of the transfer function derivation of Figure 4.54(a) is shown below.

$$I_1 = \frac{V_{in} - V_1}{R_1} = I_2 + I_3 = \frac{V_1 - V_2}{R_2} + (V_1 - KV_2)sC_1$$

$V_1 = V_2(1 + R_2C_2S)$ and $V_{out} = KV_2$ re-arranging these:

$$\frac{V_{out}}{R_{in}} = \frac{K \times 1/(R_1R_2C_1C_2)}{s^2 + [1/R_1C_1 + 1/R_2C_1 + (1-K)/R_2C_2]s + 1/(R_1R_2C_1C_2)}$$

Thus $d.\omega_o = [1/R_1C_1 + 1/R_2C_1 + (1-K)/R_2C_2]$

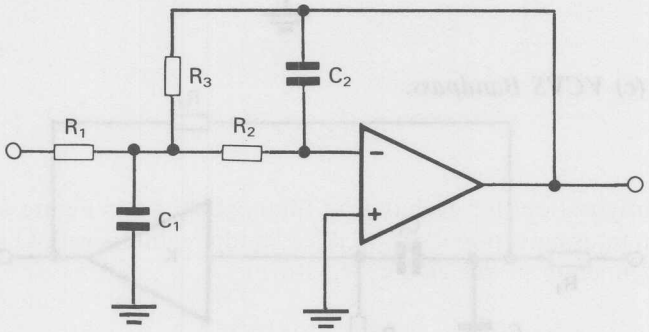
and $\omega_o^2 = 1/R_1R_2C_1C_2$

As will be shown below some simplifying assumptions can be made to make filter design easier.

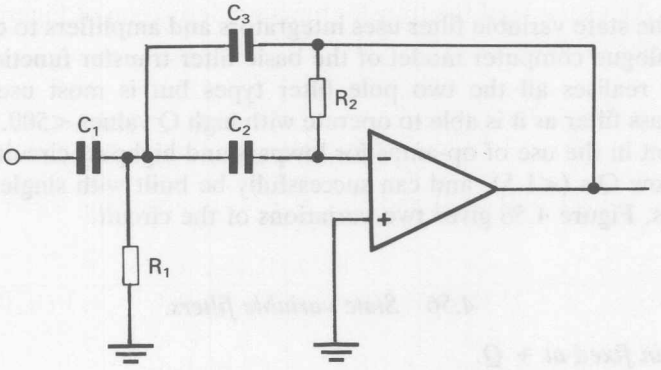
Infinite Gain Multiple Feedback (MFB) Circuits

Fig. 4.55 Multiple feedback (MFB) filters.

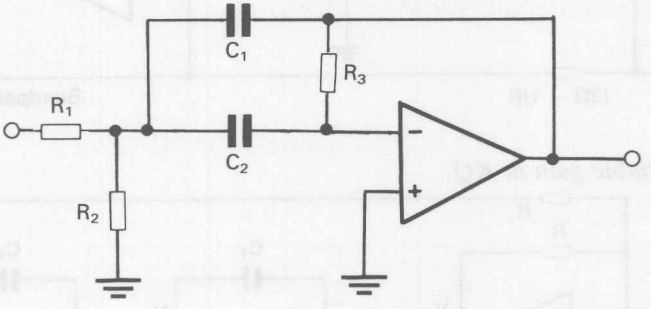
(a) MFB lowpass.



(b) MFB highpass



(c) MFB Bandpass.



Configurations for each type of filter are shown in Figure 4.55. The MFB circuit is most popularly used for bandpass filters with Q's <5, the transfer function of this (Figure 4.55(c)) is:

$$\frac{V_{out}}{V_{in}} = \frac{-s(1/R_1C_1)}{s^2 + s(1/R_3)(1/C_1 + 1/C_2) + (1/R_3C_1C_2)(1/R_1 + 1/R_2)}$$

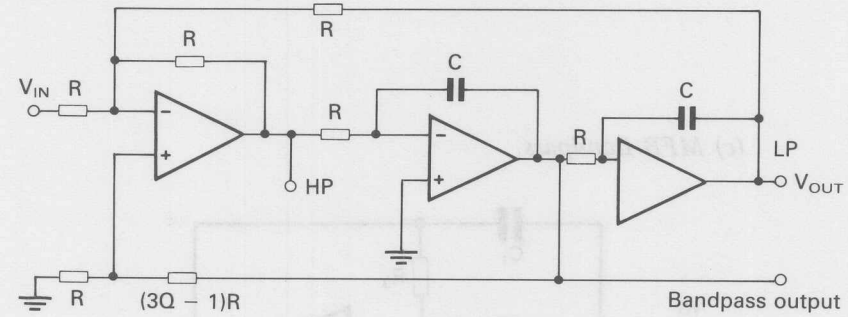
$$\frac{\omega_o}{Q} = (1/R_3)(1/C_1 + 1/C_2) \;\&\; \omega_o{}^2 = (1/R_3C_1C_2)(1/R_1 + 1/R_2)$$

State Variable Circuit

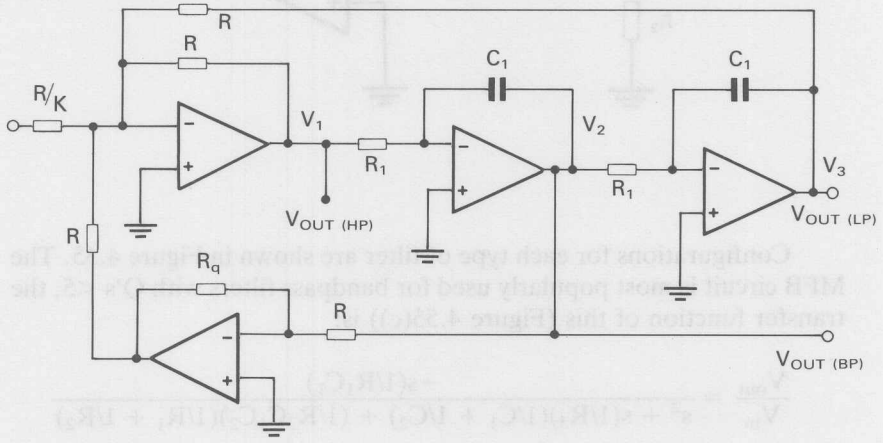
The state variable filter uses integrators and amplifiers to construct an analogue computer model of the basic filter transfer functions. The circuit realises all the two pole filter types but is most useful as a bandpass filter as it is able to operate with high Q values <500. It is less efficient in the use of op-amps for lowpass and highpass circuits, which have low Q's (<1.5), and can successfully be built with single op-amp circuits. Figure 4.56 gives two variations of the circuit.

4.56 State variable filters.

(a) Gain fixed at + Q.



(b) Variable gain at KQ.



Analysing the circuit of Figure 4.56(b) gives:

$$V_1 = -\left(K.V_{in} - V_2.\frac{R_q}{R} + V_3\right) \quad \ldots\ldots (1)$$

$$V_2 = -\frac{V_1}{sR_1C_1} \quad \ldots\ldots (2)$$

$$V_3 = -\frac{V_2}{sR_1C_1} \quad \ldots\ldots (3)$$

substituting in (2) for a bandpass response gives:

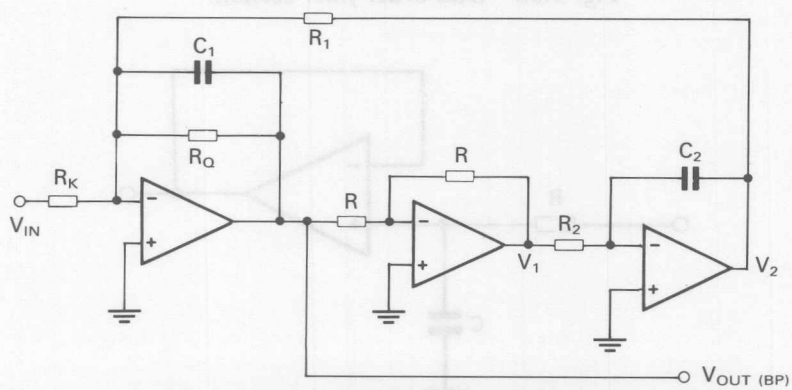
$$\frac{V_{out\ (BP)}}{V_{in}} = \frac{-K \times s(1/R_1C_1)}{s^2 + s(R_q/R)(1/R_1C_1) + 1/(R_1C_1)^2}$$

Transfer functions for lowpass and highpass can be similarly generated from equations (1) to (3).

Biquad

This is a circuit that realises a bandpass filter, but has a poor lowpass performance and no highpass output at all. It has at first sight a resemblance to the State Variable Filter but is actually different as the damping is applied by means of a resistor across the first integrator.

Fig. 4.57 Biquad bandpass filter.



The analysis of the circuit shown in Figure 4.57 is given below:

$$C_1 \text{ in parallel with } R_Q = \frac{R_Q}{1 + sC_1R_Q} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V_2 = V_{out} \cdot \frac{1}{sC_2R_2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$V_{out} = -\left(V_{in} \times \frac{R_Q}{R_K(1 + sC_1R_Q)} + V_2 \times \frac{R_Q}{R_1(1 + sC_1R_Q)}\right) \quad . (3)$$

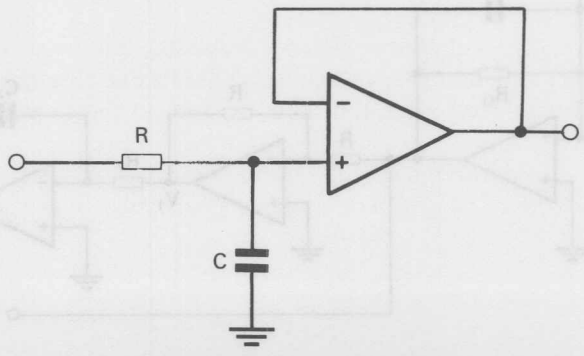
Substituting for V_2 and re-arranging:

$$V_{out} = -\frac{R_Q}{R_K} \times \frac{s(1/C_1R_Q)}{s^2 + s(1/C_1R_Q) + (1/R_1R_2C_1C_2)}$$

thus $\omega_o^2 = (1/R_1R_2C_1C_2)$ and $\omega_o/Q = (1/C_1R_Q)$.

In summary all these circuit topologies assume that the source impedance is low and provides, where necessary, the appropriate level of d.c. bias. This is most effectively achieved by use of a suitable biased voltage follower to buffer the filter input. A simple RC voltage divider may be used at the input of the voltage follower to produce an odd order filter section with $\omega_o = (1/RC)$. (See Figure 4.58).

Fig. 4.58 Odd order filter section.



Filter Normalization and Scaling

The filter Tables 4.2 and 4.3 give pole positions that produce filters normalised to 1 ohm and 1 radian/second with cut-off at −3dB. To produce a usable filter these values have to be scaled for impedance Z and frequency ω_c. To scale a filter to impedance Z all resistor values are multipled by Z and all capacitor values are divided by Z (i.e. $ZX_c = (Z \times 1/(\omega C) = 1/(\omega C/Z)$; this assumes a normalised impedance of 1 ohm. Where a filter already is at impedance z the factor is Z/z. To scale a filter to frequency f_c all capacitor values are divided by $2\pi f_c$ (which equals ω_c the cut-off frequency of the whole filter); this gives a smaller value of capacitor with the same impedance at a higher frequency.

Cascaded Sections

The basic building blocks of single and two pole filter sections are cascaded to form higher orders of filter. Greatest input signal dynamic range and prevention against op-amp saturation by high amplitude signals, particularly at the band edge, is achieved by cascading sections in order of decreasing damping (increasing Q) with the first section having the highest damping (lowest Q).

Op-amp Effects on Filter Performance

Gain-bandwidth and slew rate will limit the accuracy and highest frequency of operation for a given filter realisation. As the filter gain-cut-off frequency product approaches the op-amp gain-bandwidth product the accuracy of the cut-off frequency will be reduced. Closed loop phase shift under similar conditions will cause Q enhancement. To limit these effects open loop gain over closed loop gain should be >10 at the filters cut-off frequency. For filters made from integrators the open loop gain should be $>5\times Q$.

Slew-rate limits the large signal bandwidth, but more subtly it can effect stability with increasing amplitude. This is due to additional phase shift being introduced when the signal is close to the slew limit.

These considerations should be taken into account when choosing the bias mode of a LinCMOS op-amp for a particular filter specification.

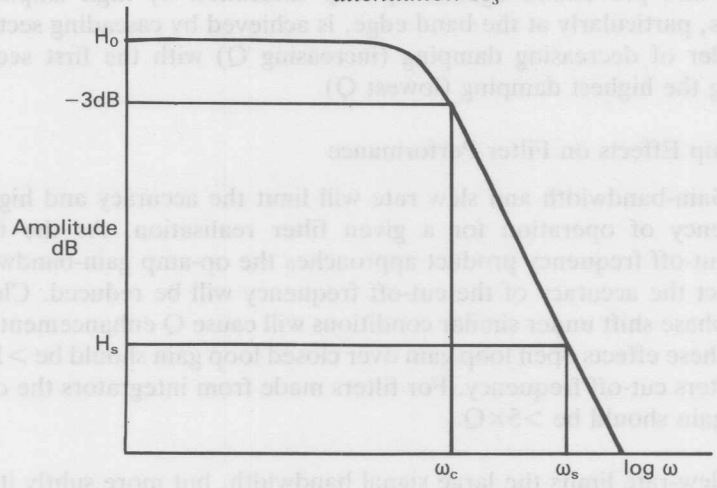
Filter Design Examples

General Design Steps

1. Determine the most important filter characteristic required in terms of amplitude, group delay (phase linearity) or transient response. Choose the most appropriate filter transfer function or by default use the Butterworth response as this gives the best overall compromise.

2. Determine the order n of the filter required in terms of the lowpass response. Figure 4.59 shows slope factor ω_s/ω_c at attenuation H_s. This can be used directly in the above equation (page 4–37) for Butterworth or from Figures 4.48 or 4.51 for Chebyschev or Bessel.

Fig. 4.59 Determination of slope factor $\frac{\omega_s}{\omega_c}$ *at attenuation* H_s.



3. Determine the number of sections needed to implement the filter. Each 2nd order section gives order n = 2 for low or highpass filters and order n = 1 for bandpass filters.

4. Determine the d (or Q) and ω_o for each section from the poles positions of Table 4.2 or 4.3.

5. Determine the circuit topology to be used taking d or Q values

and sensitivities into account. VCVS are the first choice for lowpass and highpass filters (low Q). For bandpass filters MFB are used for low Q <5 and state variable for higher value Q's.

6. Translate d or Q and ω_o values into circuit component values by comparing the standard filter transfer function with the chosen circuit transfer function and making simplifications where possible. The most general of these is to equate all R's and C's.

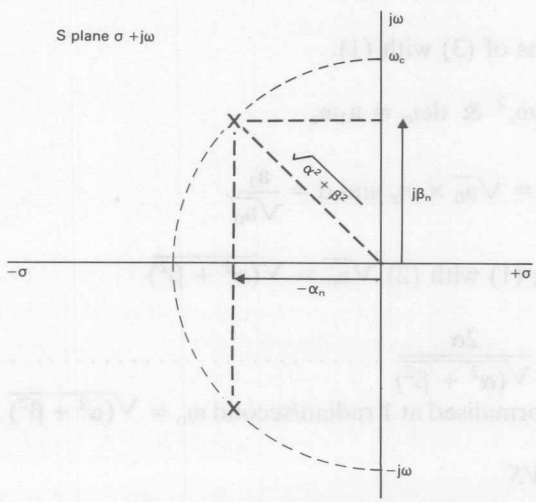
7. Scale the normalised 1 ohm and 1 radian/second values for the operating impedance and −3dB cut-off frequency ω_c. The choice of impedance may be implied by starting with standard value capacitors (see example below).

Lowpass Filter Design Examples

Determination of d and ωo from pole positions

The arrangement of pole positions $\alpha_n \pm j\beta_n$ (Figure 4.60) determines a filters frequency and phase response.

Fig. 4.60 Pole–zero diagram for 2nd order lowpass section.



Damping d or 1/Q and ω_o can be determined in terms of these as shown below:

Filter section two pole response can be expressed in terms of overall filter cut-off frequency ω_c, where coefficients a_0 & a_1 modify these for filter sections:

$$H(s) = \frac{a_0\omega_c^2}{s^2 + sa_1\omega_c + a_0\omega_c^2} \quad \ldots\ldots (1)$$

In terms of pole positions:

$$= \frac{s_1s_2}{(s - s_1)(s - s_2)} = \frac{s_1s_2}{s^2 - (s_1 + s_2)s + s_1s_2}$$

where $s_1 = -\alpha + j\beta$ and $s_2 = -\alpha - j\beta$

$$\therefore H(s) = \frac{(\alpha^2 + \beta^2)\omega_c^2}{s^2 + 2\alpha\omega_c s + (\alpha^2 + \beta^2)\omega_c^2} \quad \ldots\ldots (2)$$

Using the standard form in terms of d or 1/Q and ω_o (where ω_o is the filter section cut-off):

$$H(s) = \frac{\omega_o^2}{s^2 + d\omega_o s + \omega_o^2} \quad \ldots\ldots (3)$$

equating terms of (3) with (1).

$$\omega_o^2 = a_0\omega_c^2 \;\&\; d\omega_o = a_1\omega_c$$

Then $\omega_o = \sqrt{a_0} \times \omega_c$ and $d = \dfrac{a_1}{\sqrt{a_0}}$

by comparing (1) with (2) $\sqrt{a_0} = \sqrt{(\alpha^2 + \beta^2)}$

$$\& \therefore d = \frac{2\alpha}{\sqrt{(\alpha^2 + \beta^2)}} \quad \ldots\ldots (A)$$

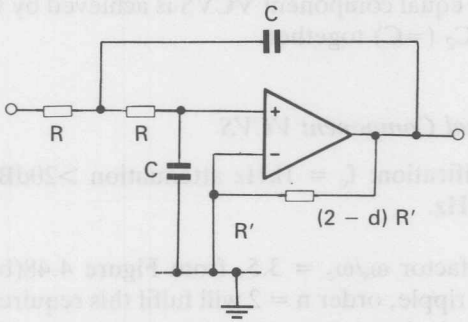
For ω_c normalised at 1 radian/second $\omega_o = \sqrt{(\alpha^2 + \beta^2)}$ . . . . . (B)

Lowpass VCVS

$$d\omega_o = [1/R_1C_1 + 1/R_2C_1 + (1 - K)/R_2C_2] \;\&\; \omega_o^2 = 1/R_1R_2C_1C_2$$

Figure 4.61 gives equal component case $R_1 = R_2 = R$; $C_1 = C_2 = C$ $d\omega_o = (3 - K)/RC$; $\omega_o = 1/RC$; $\therefore d = (3 - K)$ giving gain setting resistors R′ and R′ (2 − d).

Fig. 4.61 Equal-component VCVS lowpass filter.



A Butterworth filter 2nd order (n = 2) has $\alpha = -0.7071$, $\beta = \pm 0.7071$ from Table 4.2. The above equations (A) & (B) gives $\omega_o = 1$ and $d = 1.4142$.

With a filter specification of $f_c = 1$ kHz and impedance Z = 10kohms. An attenuation of 24dB exists at 4kHz (calculated from the Butterworth attenuation equation page 4–37). Scaling for impedance and frequency using $\omega_o = 1/R_n.C_n$ (where suffix n indicates values normalised to 1 ohm and 1 rad/sec), for some chosen value of capacitor C then:

$$C = C_n \times \frac{1}{\omega_c Z} = C_n \times \frac{1}{2\pi \times 10^3 \times 10^4} = C_n \times 15.9 \times 10^{-9}$$

choose C = 2.2nF $\therefore C_n = 2.2/15.9 = 0.1382$

$R_n = \omega_o/C_n = 1/0.1382 = 7.234$ and scaled to 10 kohms = 72.34 kohms. This result can be achieved directly from

$$R_n = \frac{1}{\omega_o C_n}; C = \frac{C_n}{\omega_c Z} \quad \text{gives } R = [R_n Z] = \frac{1}{\omega_o \omega_c C}$$

where R is the resistor value resulting from choosing C. Normalised

filter section cut-off frequency ω_o is seen to be a scaling factor for actual filter-cut-off frequency ω_c.

Gain setting resistors (referring to Figure 4.61): R′ & R′ (2 − d) = R′ (0.5858) giving typical values of 200k and 117.2kohm (120k).

Tuning the equal component VCVS is achieved by varying R_1 & R_2 (=R) or C_1 & C_2 (=C) together.

Chebyshev Equal Component VCVS

Filter specification: f_c = 1kHz attenuation >20dB at 3.5kHz and <1.5 dB at 800Hz.

The slope factor ω_s/ω_c = 3.5, from Figure 4.48(b) of Chebyshev filters with 1dB ripple, order n = 2 will fulfil this requirement. Damping d and ω_o are calculated from the pole positions of Table 4.3 using equations (A) & (B): d = 1.0455 and ω_o = 0.8623. If C is chosen as above to be 2.2nF then $R = 1/(\omega_o\omega_c C)$ = 83.9 kohms. Gain setting resistors R′ & R′ (2 − d) = 0.9545R′ typically both 100k's for practical purposes.

For higher orders of filter the process is repeated for each section. Suitable values of capacitor or impedance are chosen independently for each section.

Chebyshev VCVS Fourth Order

Filter specification: f_c = 1kHz, attenuation >60dB at 4kHz and <1dB at 800Hz. From Figure 4.48(b) of 1dB responses a 4th order is seen to fulfil this requirement, as ω_s/ω_c = 0.8 and 4. Two 2nd order sections are needed to realise this filter with d_1 = 1.2746, ω_{o1} = 0.50195 and d_2 = 0.28094, ω_{o2} = 0.94325 calculated using equations A & B from the pole positions Table 4.3.

Using the equal component VCVS circuit: scaling for impedance by reason of the value of capacitor chosen (that is choosing C = C_1 = C_2 = 2.2nF) and scaling for frequency $2\pi f_c$:

$$R_1 = \frac{1}{\omega_c\omega_o C} = 144\text{kohms (150k) similarly } R_2 = 76.7\text{kohms (75k)}$$

Gain setting resistors R_1' & $R_1'(2-d) = R_1'(0.7254)$ (typ 200k & 150k).

Gain setting resistors R_2' & $R_2'(2-d) = R_2'(1.7190)$ (typ 130k & 220k).

Bessel VCVS Fourth Order

Bessel filters can be used to provide a constant delay to a signal. As can be seen from Figure 4.49 for n = 4 a flat delay extends up to the cut-off frequency. From the pole positions of Table 4.2(b) $d_1 = 1.91595$, $\omega_{o1} = 1.41924$ and $d_2 = 1.2415$, $\omega_{o2} = 1.591124$ using equations (A) & (B). Then for the equal component VCVS again choosing C = 2.2nF, R_1 = 51kohm $R_1'(2-d) = R_1'(0.084)$ (100k & 8.2k), R_2 = 47kohm $R_2'(2-d) = R_2'(0.7852)$ (100k & 75k).

Unity Gain VCVS

Another popular simplification of the lowpass VCVS transfer function is to make K = 1 i.e. unity gain. (This gives a filter with the widest possible bandwidth).

$$\text{Thus } d\omega_o = \frac{1}{R_1C_1} = \frac{1}{R_2C_1}$$

$$\text{putting } R_1 = R_2 = R; \quad d\omega_o = \frac{2}{RC_1}$$

$$\text{and } \omega_o^2 = \frac{1}{R_1R_2C_1C_2} = \frac{1}{R^2C_1C_2};$$

$$\text{thus } C_1 = \frac{2}{Rd\omega_o} \;\&\; C_2 = \frac{d}{2R\omega_o}$$

$$\& \; \frac{C_1}{C_2} = \left(\frac{2}{d}\right)^2$$

e.g. for a 2nd order Butterworth Filter d = 1.4142 & ω_o = 1 choose C_2 = 2.2nF $C_1 = C_2(2/d)^2 = 2 \therefore C_1$ = 4.4nF.

Impedance scaling (by capacitance choice) and frequency scaling to f_c = 1kHz $R = 1/(\omega_o\omega_c dC_1)$ = 51kohms.

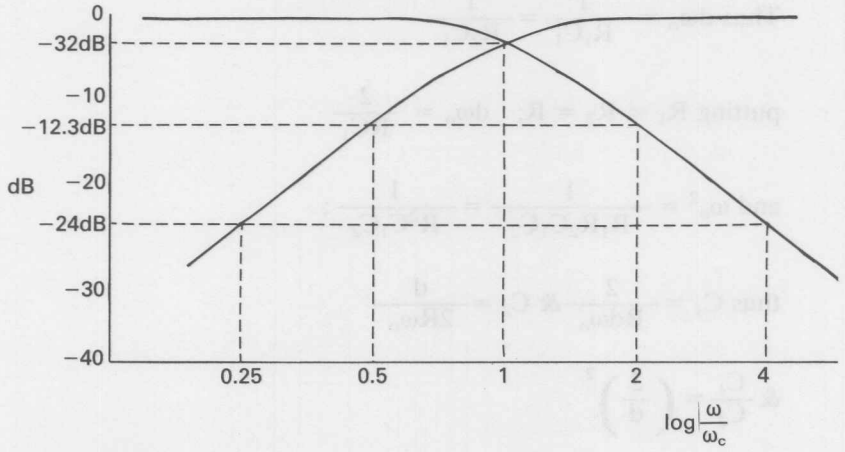
This circuit can be tuned by varying R_1 & R_2 together and by varying C_1 & C_2 if their ratio $(d/2)^2$ is maintained.

Other unity gain (K = 1) simplifications such as: a) $C_1 = C_2 = C$ & b) $R_1.C_1 = R_2C_2$ i.e. $a = C_1/C_2 = R_2/R_1$ yield complex interdependence between circuit variables and complicated tuning.

Highpass Filters

With the proviso that a true active highpass filter cannot be produced because finite op-amp gain-bandwidth limits the high frequency performance, designing such a filter is a relatively straight forward matter. It is achieved by transposing a highpass into a lowpass design by replacing normalised frequencies f of the highpass requirement into normalised frequencies l/f of a lowpass 'prototype' (see Figure 4.62). A lowpass filter is thus designed and then components (R's & C's) for a typical VCVS topology are then interchanged to give the highpass filter.

Fig. 4.62 Typical normalised highpass – lowpass transformation.



Using the lowpass Butterworth n = 2 (page 4–57) example above, ω_s/ω_c at −24dB = 4, this is equivalent to $\omega_s/\omega_c = 0.25$ (250Hz for f_c = 1kHz) for the highpass transposition. Thus a highpass filter with

f_c = 1kHz and −24dB at 250Hz is produced by putting the lowpass circuit values in the circuit configuration of Figure 4.54(b).

To achieve the widest bandwidth the unity gain VCVS configuration should be used along with the high bias mode LinCMOS op-amps. Wide bandwidth bandpass filters that are made up of cascaded lowpass and highpass sections give one of the best uses of this type of high pass filter.

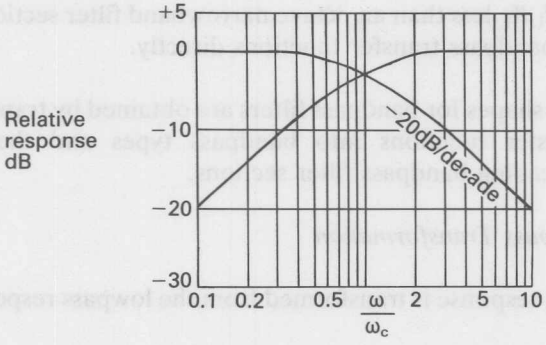
Bandpass Filters Design Examples

Introduction

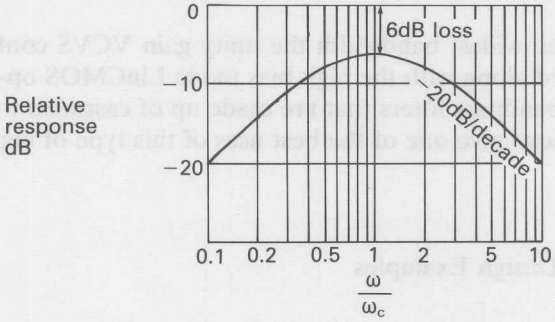
Bandpass filters can be divided into two types distinguished by the ratio of upper (f_U) to lower (f_L) −3dB cut-off frequency. When this ratio exceeds approximately 2 (an octave) the filter is a wideband type and is implemented by cascading highpass and lowpass sections. The criteria for wideband filters can also be expressed in terms of centre frequency f_r ($= \sqrt{f_U f_L}$) and bandwidth ($BW = f_U - f_L$) where $BW/f_r \leq 0.7$ ($= 1/Q$ for a single 2 pole section). Figure 4.63 gives a comparison between wideband and narrowband for $f_U/f_L < 2$, showing a loss for wideband and Q magnification for narrowband.

Fig. 4.63 Wideband filter limitations.

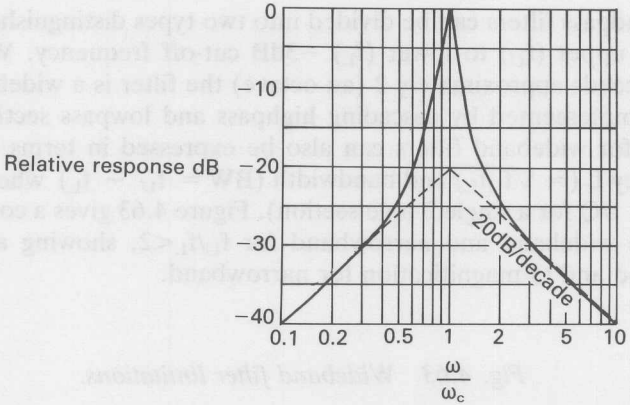
(a) Individual low & highpass responses.



(b) Sum of low & highpass responses showing loss.



(c) Narrow band single pole response with Q = 10.



For ratios of f_U/f_L less than an octave narrowband filter sections are used that realise bandpass transfer functions directly.

The response shapes for bandpass filters are obtained by transforming lowpass transfer functions into bandpass types and then implemented by cascading bandpass filter sections.

Lowpass to Bandpass Transformation

The bandpass response is transformed from the lowpass response as follows:

The normalised lowpass transfer function $H(s) = \dfrac{1}{S + 1}$

is transformed into bandpass by substitution of:

$$S = \frac{1}{BW}\left(\frac{s^2 + \omega_r^2}{s}\right) \text{ to give:}$$

$$H(s) = \frac{s\omega_r/Q}{s^2 + s\omega_r/Q + \omega_r^2}$$

Where $Q = \frac{\omega}{BW}$ and ω is the centre frequency.

(S and s are both complex variables.)

(ω_r is used here to differentiate from ω_c and ω_o, the low and highpass overall filter and section −3dB cut-off frequencies respectively.)

This transformation can be described in terms of a pole-zero diagram, as shown in Figure 4.64, where a single low frequency pole is transformed to give a pair of conjugate poles and a zero at the origin. The transformation above, by definition, transforms the lowpass bandwidth ω_c into the bandpass bandwidth as shown.

Fig. 4.64 Single pole lowpass to bandpass transformation.

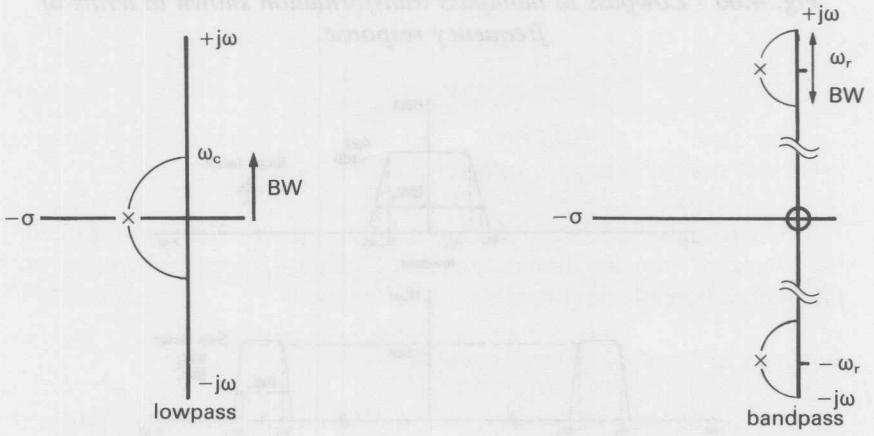


Figure 4.65 show this transformation for a multi-pole response and Figure 4.66 shows the same in terms of filter amplitude response.

Fig. 4.65 Multiple lowpass to bandpass transformation.

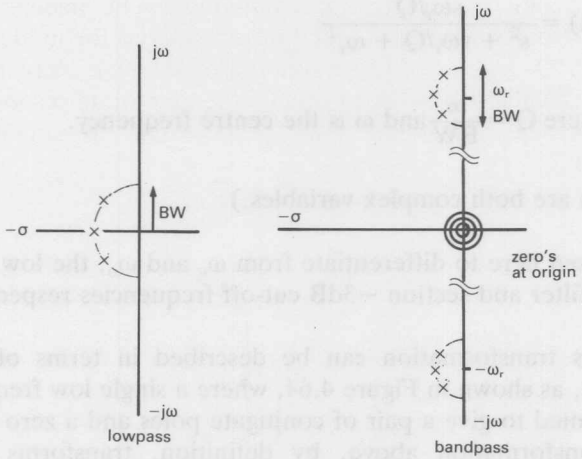
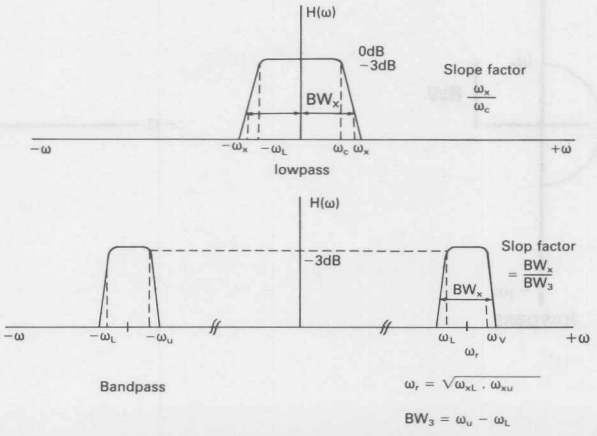


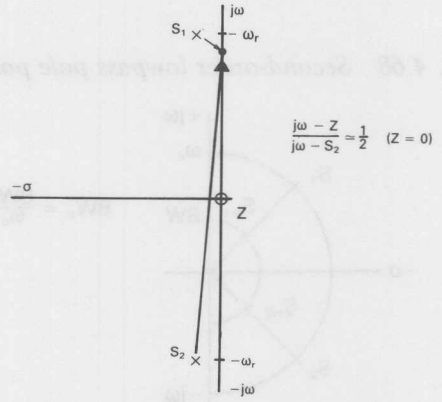
Fig. 4.66 Lowpass to bandpass transformation shown in terms of frequency response.



Narrowband Approximation

To obtain the amplitude and phase response from the diagrams of Figures 4.64 and 4.65 all the poles and zeros have to be taken into consideration. With increasing values of Q the poles move closer to the jω axis. Using this fact, an approximation can be made so that only the cluster of poles around ω_r need be considered for moderate and high values of Q. Values of Q>5 give reasonable and increasing accuracy. For lower values some distortion of the amplitude response will result and empirical adjustment may be necessary to obtain the desired response.

Fig. 4.67 Pole – zero diagram showing narrowband approximation.



The bandpass response expressed in terms of poles and zeros is given by:

$$H(s) = \frac{\omega_r}{Q} \times \frac{s}{(s - s_1)(s - s_2)}$$

The substitution $s = j\omega$ can be made for operation along the frequency axis.

$$H(j\omega) = \frac{\omega_r}{Q} \times \frac{j\omega}{(j\omega - s_1)(j\omega - s_2)}$$

Reference to Figure 4.67 shows that when $j\omega \simeq j\omega_r$

$$\frac{j\omega}{j\omega - s_2} \simeq \frac{1}{2} \text{ and } H(j\omega) = \frac{\omega_r}{Q} \times \frac{1}{(j\omega - s_1)} \text{ centred on } \omega_r.$$

This shows that a bandpass 2 pole (2nd order) section contributes only one pole (order) to an overall bandpass response. It also shows that lowpass poles clustered around the origin can be used to determine a new set of poles with a bandpass response. These new poles will give a bandpass bandwidth BW equal to the cut-off frequency ω_c of the lowpass poles and be centred on ω_r.

Lowpass to Bandpass pole position Transformation

Fig. 4.68 Second-order lowpass pole positions.

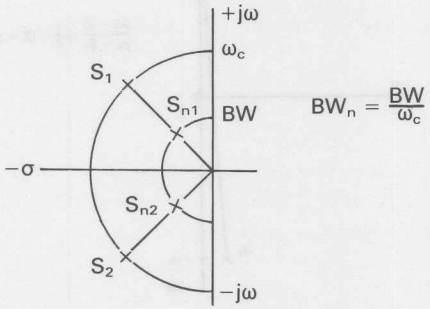
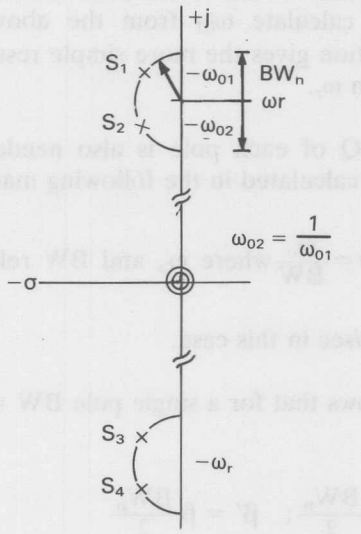


Figure 4.68 is a typical pole-zero diagram for a symmetrical pair of poles describing a 2nd order lowpass filter with cut-off ω_c. The positions of the poles $s_{1,2} = -\alpha \pm j\beta$ are proportional to the cut-off frequency ω_c. If an arbitrary cut-off called bandwidth BW ($<\omega_c$) is chosen then a normalised bandwidth will be $BW_n = BW/\omega_c$. New pole positions $s_{n1,2} = -\alpha_n \pm j\beta_n$ (where $\alpha_n = BW_n.\alpha$ and $\beta_n = BW_n.\beta$) exist for this BW_n, thus the new pole positions are $s_{n1,2} = BW_n.(-\alpha \pm j\beta)$. Figure 4.69 shows these pole transformed into the bandpass case with centre frequency ω_r normalised to 1 rad/sec.

Fig. 4.69 Normalised bandpass transformation.



BW_n = normalised −3dB bandwidth
ω_r = centre frequency normalised to 1 rad/sec

It can be seen that the radius of the circle upon which they lie has further contracted to $BW_n/2$ to give an overall bandpass bandwidth of BW_n. From the diagram the positions of all the poles (both $+\omega_r$ & $-\omega_r$) can be seen to be:

$$s_{1,2,3,4} = -\alpha \frac{BW_n}{2} \pm j\left(1 \pm \beta \frac{BW_n}{2}\right)$$

The poles of interest in the narrowband approximation are:

$$s_{1,2} = -\alpha \frac{BW_n}{2} + j\left(1 \pm \beta \frac{BW_n}{2}\right)$$

Using this equation the normalised pole positions from the origin i.e. the value of frequency for each bandpass section are given by:

$$\omega_{o1,2} = \sqrt{\left(\frac{\alpha BW_n}{2}\right)^2 + \left(1 \pm \frac{\beta BW_n}{2}\right)^2}$$

Where, as in the lowpass case, ω_o can be considered as a frequency scaling factor, this time to the normalised centre frequency ω_r. It is only necessary to calculate ω_{01} from the above equation, as the original transformation gives the more simple result $\omega_{o2} = 1/\omega_{o1}$ for a pole pair centred on ω_r.

The value of Q of each pole is also needed for the bandpass realisation and this calculated in the following manner:

By definition $Q = \frac{\omega_o}{BW}$ where ω_o and BW relate to a single pole normalised to 1 rad/sec in this case.

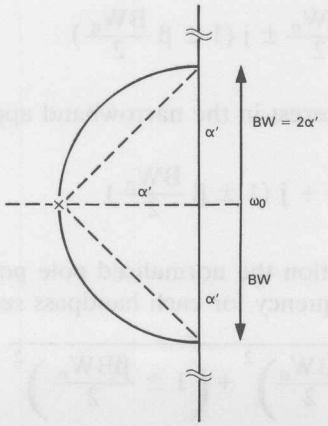
Figure 4.70 shows that for a single pole $BW = 2\alpha'$

Where $\alpha' = \alpha\frac{BW_n}{2}$; $\beta' = \beta\frac{BW_n}{2}$

From above $\omega_o = \sqrt{\alpha'^2 + (1 \pm \beta')^2}$

Thus $Q = \frac{\sqrt{\alpha'^2 + (1 + \beta')^2}}{2\alpha'}$;

Fig. 4.70 Q of a single pole.



For values of $BW_n < 0.2$ then $Q \simeq \frac{1}{2\alpha'}$

Odd orders of filter have a pole with $\beta' = 0$, $\omega_o = 1$ and $\alpha' = \alpha BW_n/2$ which is transformed from the negative real axis. For Butterworth filters the odd order pole always has a value of $\alpha = -1$. Values of α for odd order Bessel and Chebyshev filters are given in Tables 4.2(b) and 4.3 respectively.

For example a single pole filter with $f_r = 1$kHz and BW = 200Hz at −3dB would have a normalised bandwidth:

$$BW_n = \frac{BW}{\omega_r} = \frac{200}{1000} = 0.2$$

For a single pole $\alpha = -1$ and thus $\alpha' = \alpha \frac{BW_n}{2} = 0.1$

$$\therefore Q = \frac{1}{2\alpha'} = 5.$$

Thus the Q for an individual pole is obtained. (This can obtained directly from f_r/BW in this case, but this is not so for multipole filters.)

The attenuation at frequencies other than −3dB is given by manipulating the standard bandpass equation as follows:

$$H(s) = \frac{s\omega_r/Q}{s^2 + s\omega_r/Q + \omega_r{}^2};$$

Multiplying numerator and denominator by $Q/\omega_r s$ and substituting $s = j\omega$:

$$H(j\omega) = \frac{1}{1 + jQ\,(\omega/\omega_r - \omega_r/\omega)}$$

The attenuation in dB normalised to 1 rad/sec:

$$At_{dB} = -20 \log \sqrt{1 + Q^2(\omega - 1/\omega)^2}$$

where $\omega - 1/\omega$ is the bandwidth $BW = \omega_U - \omega_L$ and $\omega_r = \sqrt{\omega_U \omega_L}$

Re-arranging gives $BW = \frac{\sqrt{At^2 - 1}}{Q}$

MFB Example

Using the MFB circuit of Figure 4.55(c) the transfer function given on page 4–49 is:

$$H(s) = \frac{-s(1/R_1C_1)}{s^2 + s(1/R_3)(1/C_1 + 1/C_2) + (1/R_3C_1C_2)(1/R_1 + 1/R_2)}$$

$$\omega_o/Q = (1/R_3)(1/C_1 + 1/C_2) \;\&\; \omega_o{}^2 = (1/R_3C_1C_2)(1/R_1 + 1/R_2)$$

Where ω_o is the normalised values of ω_r.
make $C_1 = C_2 = C$

$$\therefore R_3 = \frac{2Q}{\omega_o C} \text{ and } \omega_o{}^2 = \frac{1}{C^2 R_3 R}; \quad \text{where } \frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$R = \frac{1}{2Q\omega_o C} \text{ by substitution of } R_3 \text{ and re-arranging.}$$

$$\text{Thus as } \omega_o = 1 \text{ for single pole } R_3 = \frac{2Q}{C} \quad \& \quad R = \frac{1}{2QC} = \frac{R_3}{4Q^2}$$

Choose C = 10nF and scaling for centre frequency ω_r

$$R_3 = \frac{2Q}{\omega_r C} = \frac{10}{2\pi \times 10^3 \times 10^{-8}} = 159.15 \text{ kohm (160k)}$$

$R = R_3/100 = 1.6$ kohm.

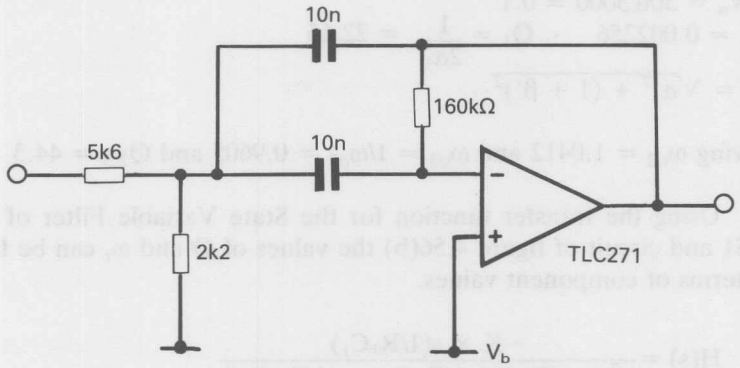
The circuit implemented using a TLC271 is shown in Figure 4.71.

$$\text{Circuit gain: at } \omega = \omega_r\text{: } H_r = \frac{-(1/R_1C)}{(2/R_3C)} = -\frac{R_3}{2R_1}$$

$$\text{Substituting for } R_3 \text{ and C: } H_r = -2Q^2\frac{R_2}{R_1 + R_2} = 13.92$$

From the requirement that the op-amp open loop gain is 10 times

Fig. 4.71 MFB bandpass filter fr = 1KHz Q = 5.



the circuit closed loop gain, a gain of >140 is needed. This sets the highest frequency at which this circuit, with the values shown, can operate. From Figure 3.16 this is approximately 20kHz for high bias mode TLC27_ LinCMOS op-amps.

When tuning the circuit for frequency the ratio of R_3 to R should be kept constant to maintain the same Q value.

Chebyshev 3 pole State Variable Filter Example

Taking as an illustrative example a filter specification of: Centre frequency f_r = 5kHz, −3dB bandwidth = 500 Hz, −40dB bandwidth = 2kHz and <1.5dB ripple, the circuit values for a State Variable circuit are calculated as follows:

$$\text{Shape factor } H_s = \frac{\text{Bandwidth at required attenuation}}{-3\text{dB Bandwidth}} = \frac{BW_x}{BW_3}$$

$$= \frac{2000}{500} = 4$$

With reference to Figure 4.48(b) a 3 pole filter with $\omega/\omega_c = 3.5$ and 1dB ripple meets the requirement.

Table 4.3 gives the pole positions as: $s_1 = -0.4513$, $s_{2,3} = -0.2257 \pm j0.8822$.

using $\alpha' = \alpha BW_n/2$ & $\beta' = \beta BW_n/2$
$BW_n = 500/5000 = 0.1$
$\alpha'_1 = 0.002256 \quad \therefore Q_1 = \dfrac{1}{2\alpha_1'} = 22.15$
$\omega_o = \sqrt{\alpha'^2 + (1 + \beta')^2}$

Giving $\omega_{o2} = 1.0412$ and $\omega_{o3} = 1/\omega_{o2} = 0.9605$ and $Q_{2,3} = 44.3$

Using the transfer function for the State Variable Filter of page 4–51 and circuit of figure 4.56(b) the values of Q and ω_r can be found in terms of component values.

$$H(s) = \frac{-K \times s(1/R_1C_1)}{s^2 + s(Rq/R)(1/R_1C_1) + (1/R_1C_1)^2}$$

$$\text{Then } \omega_r = \frac{1}{R_1C_1} \text{ and } \frac{\omega_r}{Q} = \left(\frac{Rq}{R}\right) \times \left(\frac{1}{R_1C_1}\right) \quad \therefore Q = \frac{R}{R_q}$$

and thus Q and ω_r are independently adjustable.

First section with $f_r = 5$kHz and $Q = 22.15$

$$\text{Choose } C_1 = 2.2\text{nF then } R_1 = \frac{1}{2\pi \times 5 \times 10^3 \times 2.2 \times 10^{-9}} = 14.47 \text{ kohm}$$

Choose $R = 100$k then $R_q = 100/22.15 = 4.515$ kohm

Second section: $C_1 = 2.2$nF, $R_1 = 15.06$ kohm, $R_q = 2.257$ kohm.

Third section: $C_1 = 2.2$nF, $R_1 = 13.89$ kohm, $R_q = 2.257$ kohm.

In practice when the circuit is constructed an adjustment of values may be required to allow for layout and op-amp performance. These are seen as shifts in pole frequencies and Q enhancement from the calculated values. As higher values of Q are used there will be greater the sensitivity to component tolerances. The gain of the State Variable Filter circuit is found by substituting $s = 1/R_1C_1$ in the transfer function above and gives a filter gain of KQ. An op-amp open loop gain of at least 3Q is required at the frequency of operation. The levels of input signal that can be handled are limited by the dynamic range (supply voltage and noise) and the slew rate. Using values of K less than unity

allows higher input signal amplitudes to be filtered, but does not improve the dynamic range.

This filter can be implemented using LinCMOS TLC274 high bias mode quad op-amps, and thereby utilises their larger gain-bandwidth and slew rate.

5. Application Circuit Memory Joggers

SAMPLING CIRCUITS

Fig. 5.1 Peak detector.

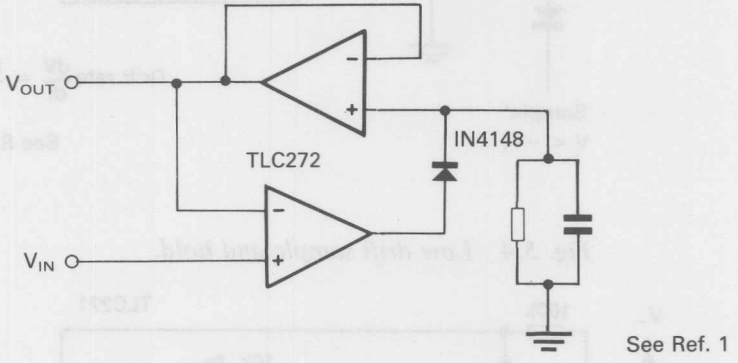


Fig. 5.2 Low drift peak detector.

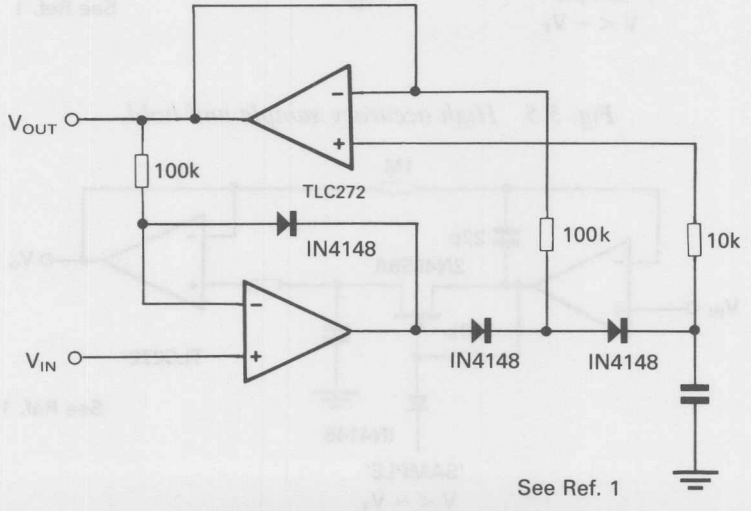


Fig. 5.3 Basic sample and hold.

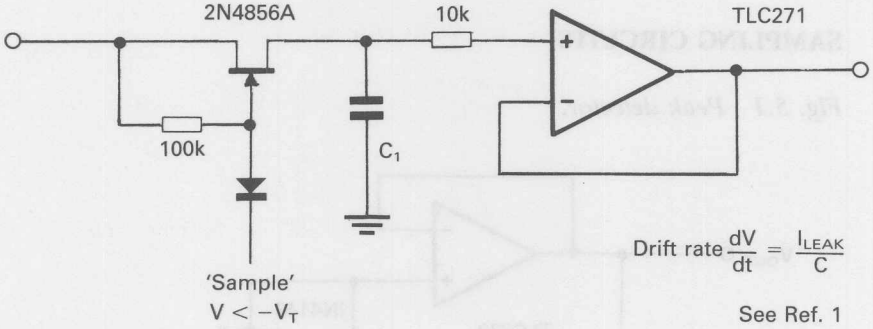


Fig. 5.4 Low drift sample and hold.

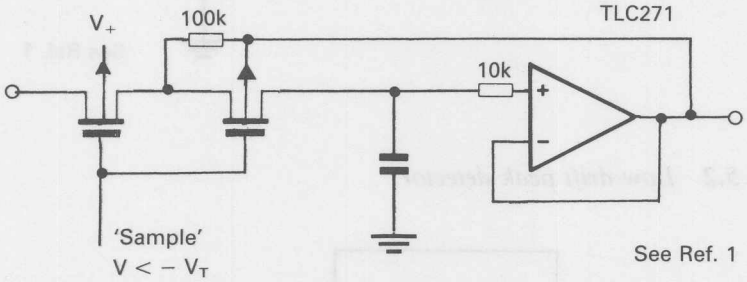


Fig. 5.5 High accuracy sample and hold.

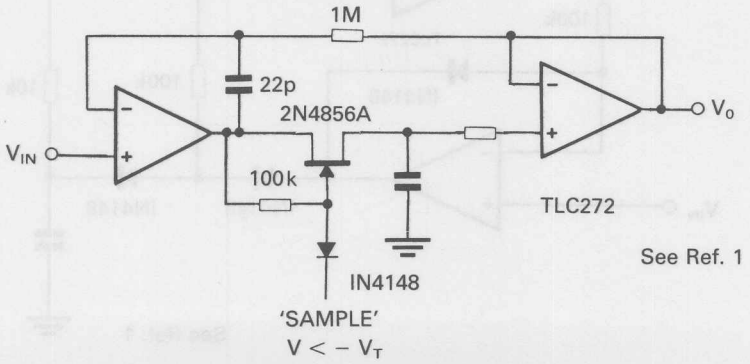
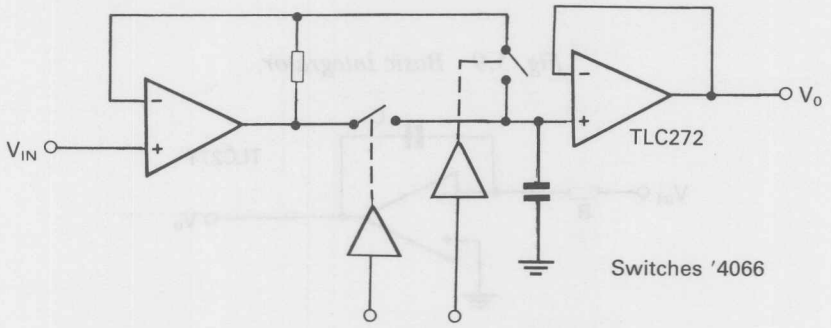


Fig. 5.6 Fast sample and hold.



RECTIFIERS

Fig. 5.7 Precision full wave rectifier (absolute value circuit).

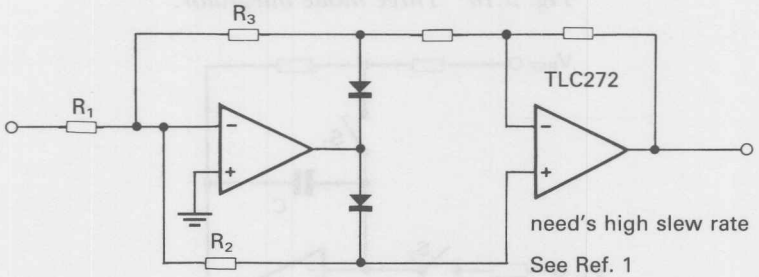
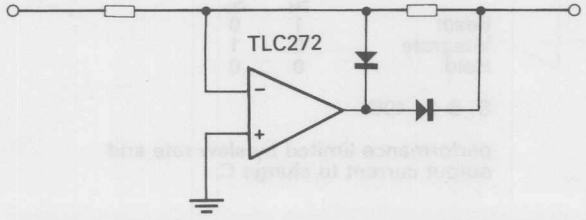
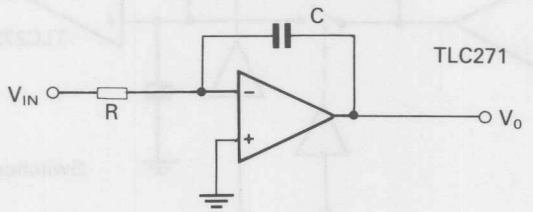


Fig. 5.8 Halfwave rectifier.



INTEGRATOR CIRCUITS

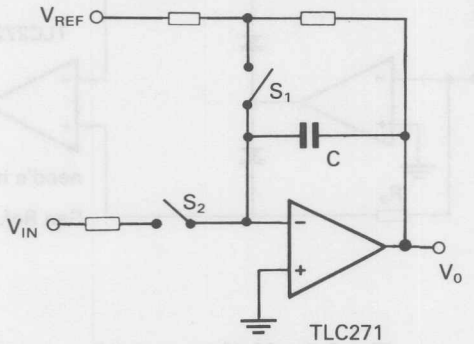
Fig. 5.9 Basic integrator.



$$V = -\frac{1}{RC}\int V_{IN}dt + \underbrace{\frac{1}{RC}\int V_{IO}dt + \frac{1}{C}\int I_{IB}dt + V_{IO}}_{\text{error terms}}$$

See Ref. 1

Fig. 5.10 Three mode integrator.

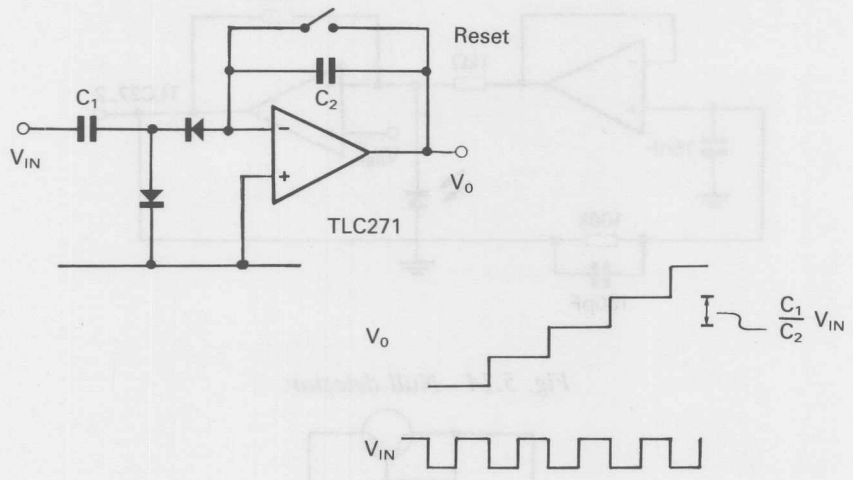


	S_1	S_2
Reset	1	0
Integrate	0	1
Hold	0	0

S_1 & S_2 4066

performance limited by slew rate and output current to charge C.

Fig. 5.11 Linear staircase generator.



AMPLIFIER CIRCUITS – LOG – PHOTO – DIODE ETC.

Fig. 5.12 Logarithmic amplifier.

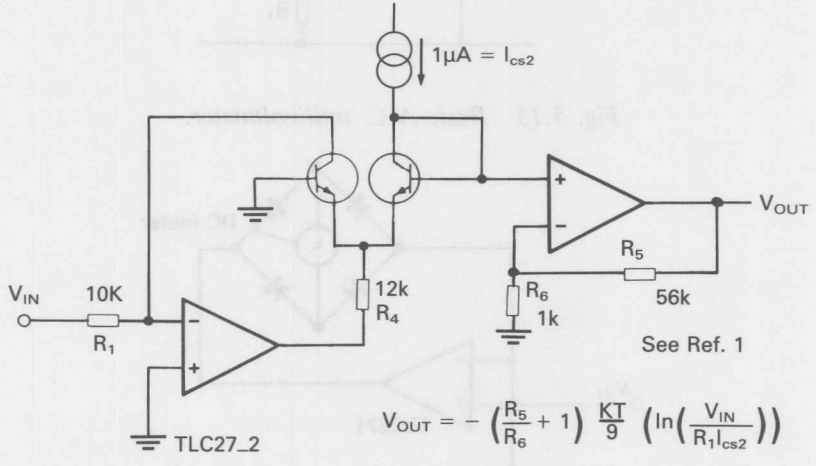


Fig. 5.13 Photo diode amplifier with ambient light rejection.

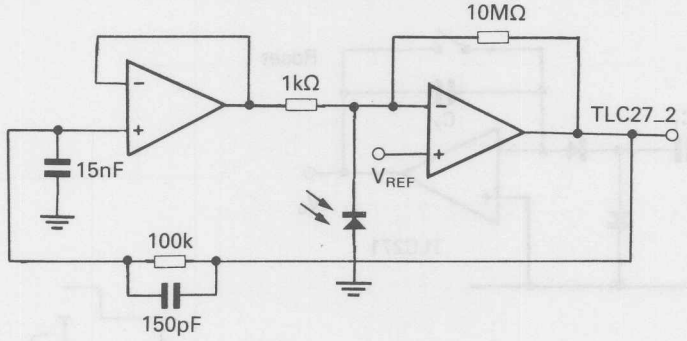


Fig. 5.14 Null detector.

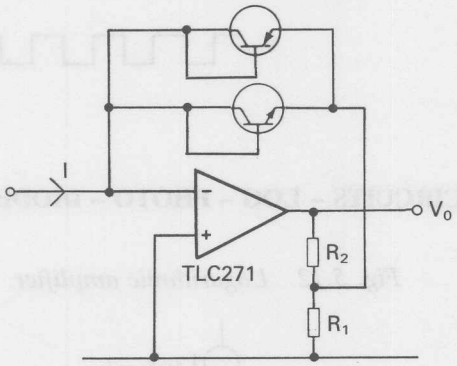


Fig. 5.15 Basic A.C. millivoltmeter.

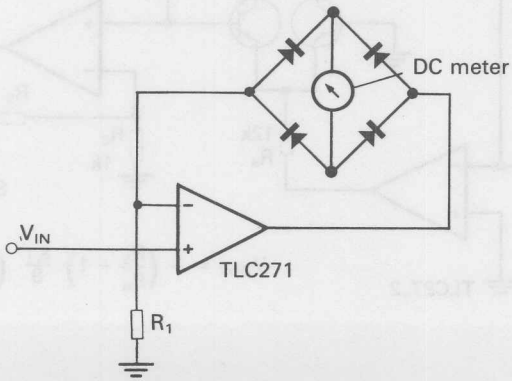


Fig. 5.16 Adder subtractor.

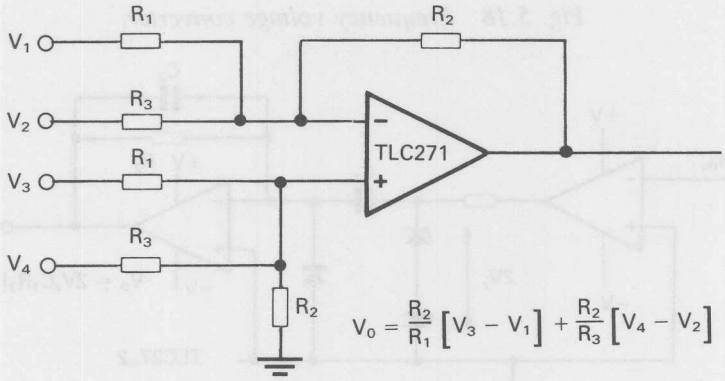
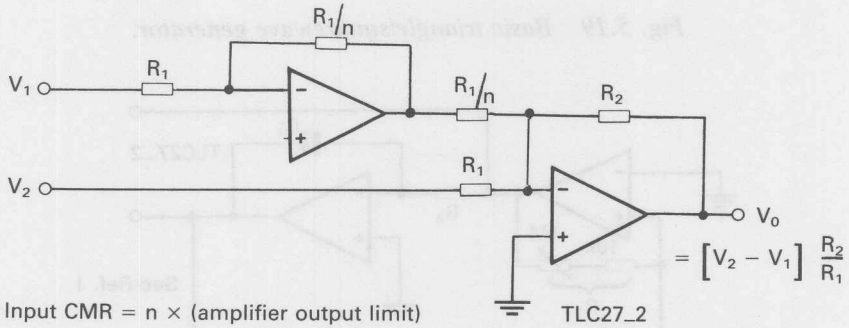


Fig. 5.17 Differential amp with high common mode rejection.



FUNCTION CIRCUITS

Fig. 5.18 Frequency voltage converter.

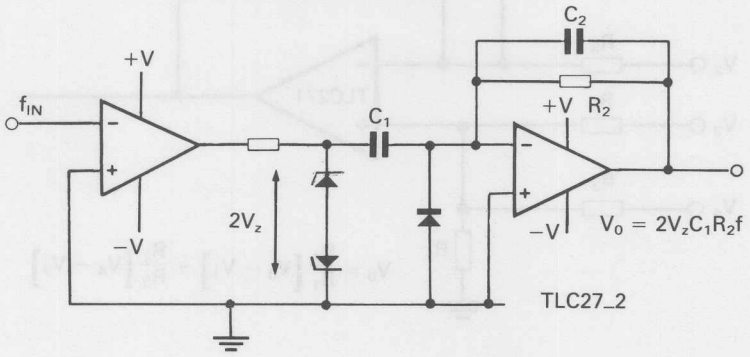
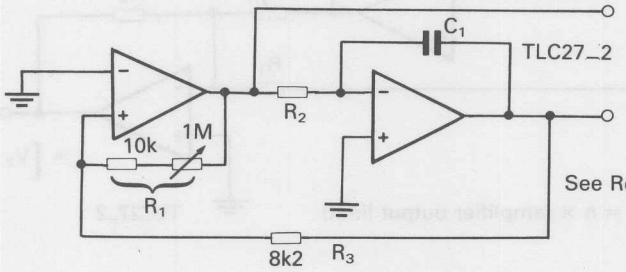


Fig. 5.19 Basic triangle/squarewave generator.



$f_{osc} = \frac{R_1}{4C_1R_2R_3}$ Integrator error $\left[\pm \frac{V_{IO}}{CR} + \frac{I_{IB}}{C}\right]$ Causes asymmetry at low frequencies, this is minimised by low I_{IB} LinCMOS & V_{IO} selections.

Fig. 5.20 Variable amplitude triangle generator.

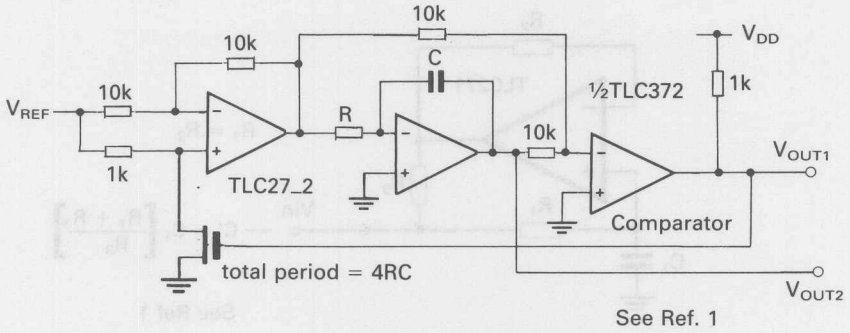


Fig. 5.21 Voltage to current converter.

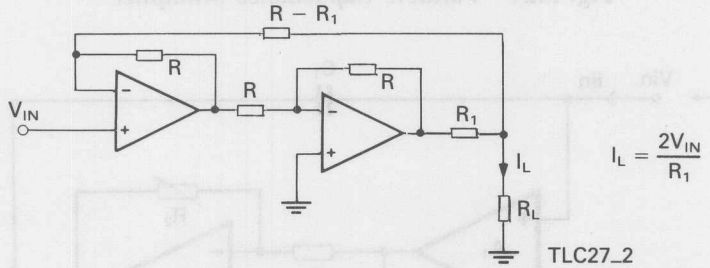


Fig. 5.22 Pulse width modulator.

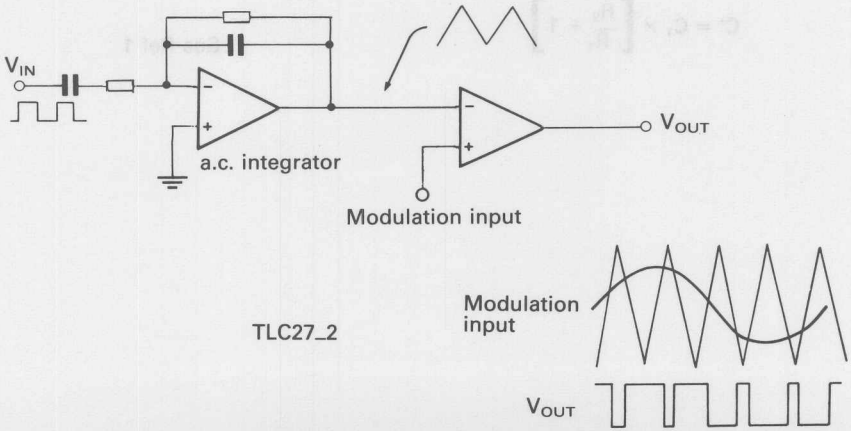


Fig. 5.23 Capacitance multiplier

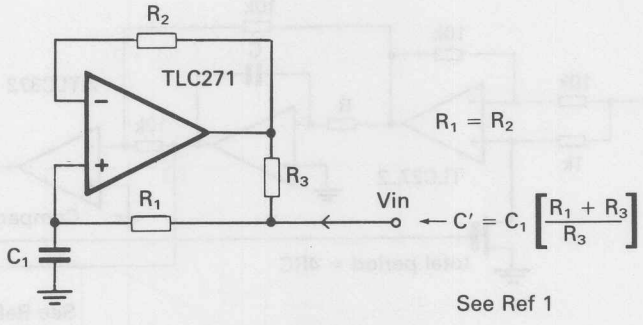
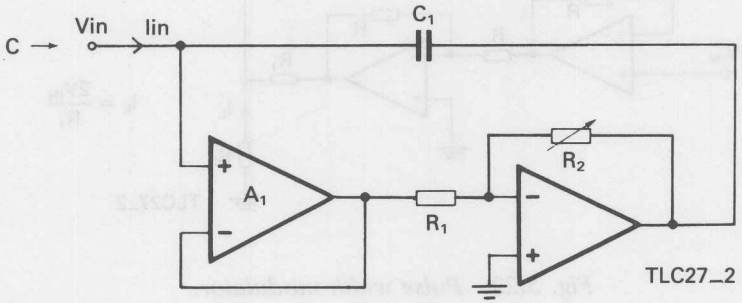


Fig. 5.24 Variable Capacitance Multiplier

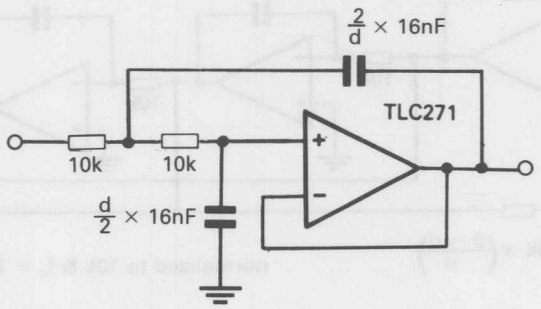


$$C' = C_1 \times \left[\frac{R_2}{R_1} + 1\right]$$

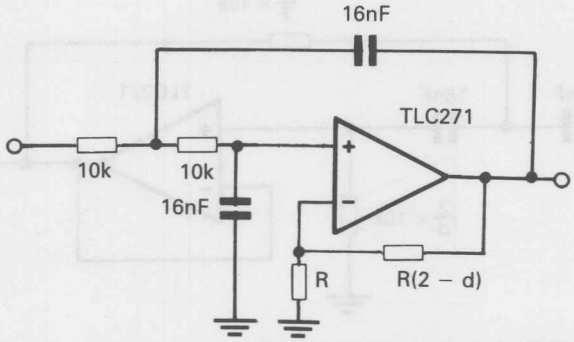
See Ref 1

FILTERS

Fig. 5.25 Lowpass VCVS.



Unity gain Sallen & Key (VCVS) normalised to: f_c = 1kHz Z = 10k ohms.



Equal component Sallen & Key, gain = +(3 – d), normalised to: f_c = 1kHz
Z = 10k ohms.

Fig. 5.26 Lowpass MFB.

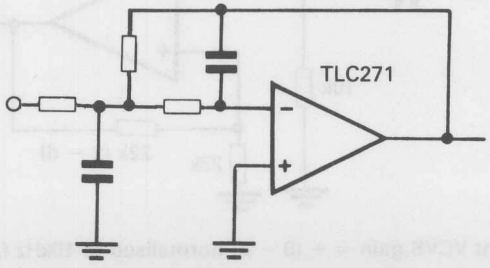


Fig. 5.27 State variable.

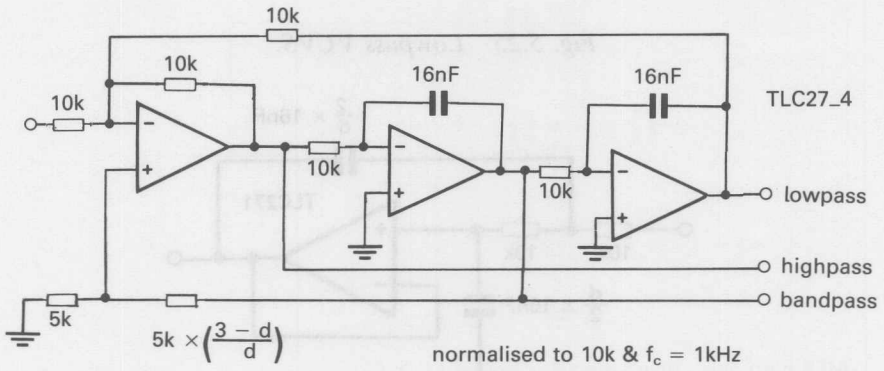
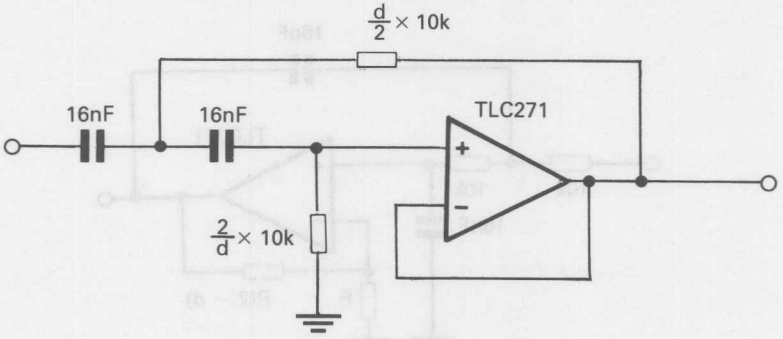
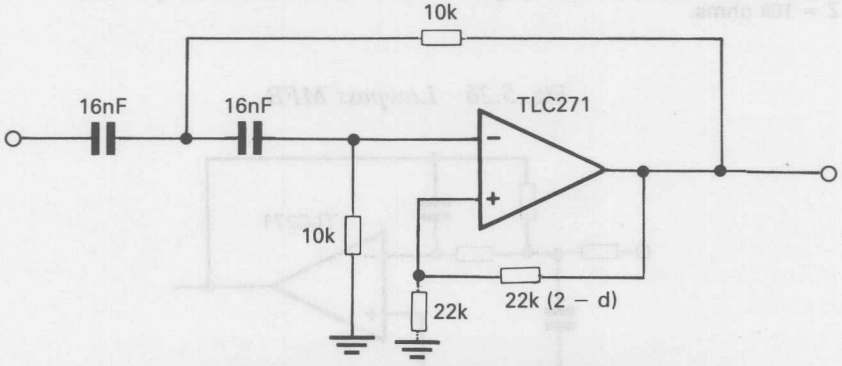


Fig. 5.28 High pass VCVS.

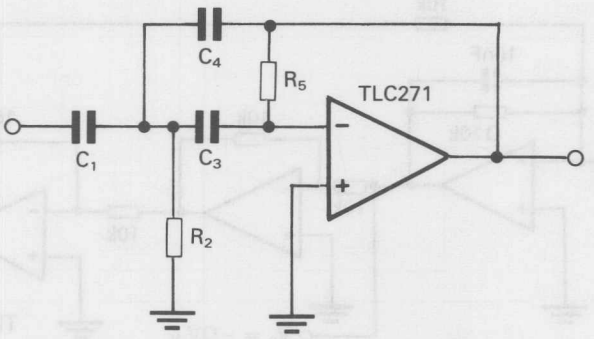


Unity gain VCVS normalised to 1kHz at 10k ohm



Equal component VCVS gain = + (3 − d) normalised to 10kHz f_i = 1kHz

Fig. 5.29 Highpass MFB.



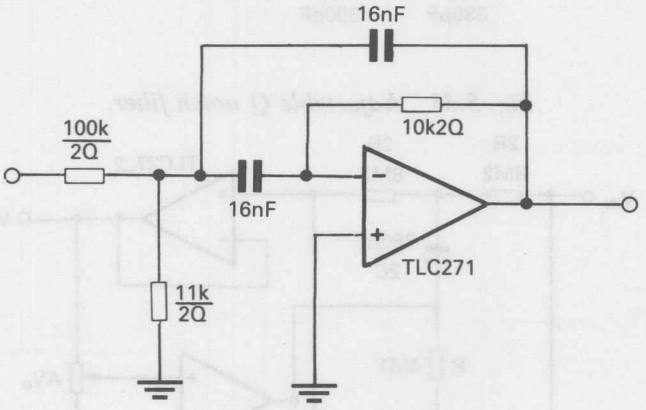
MFB high pass: given gain H_0.d, ω_0, put $C = C_1 = C_3$

$$R_5 = \frac{1}{d\omega_0 C}(2H_0 + 1),$$

$$R_2 = \frac{d}{\omega_0 C\,(2H_0 + 1)},$$

$$C_4 = \frac{C_1}{H_0}$$

Fig. 5.30 Bandpass MFB.



Normalised to 10k/ at f_c = 1kHz, Q < 5.

Fig. 5.31 Biquad.

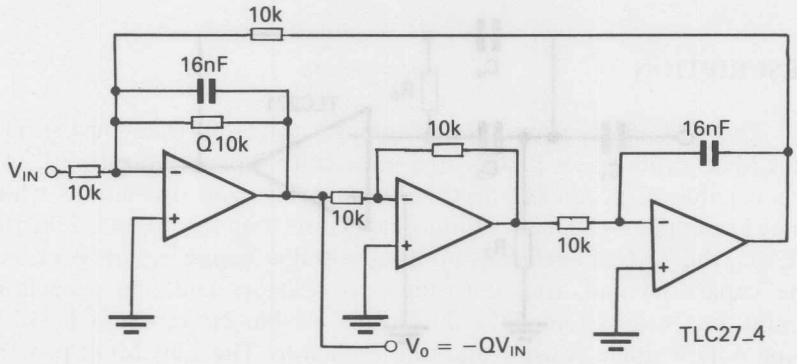


Fig. 5.32 Twin T 50Hz notch filter.

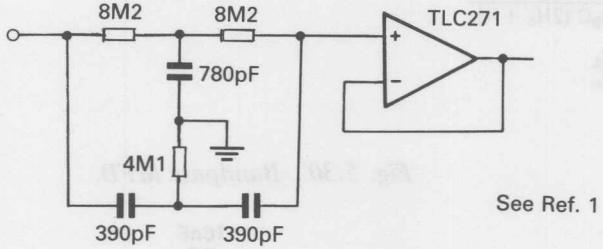
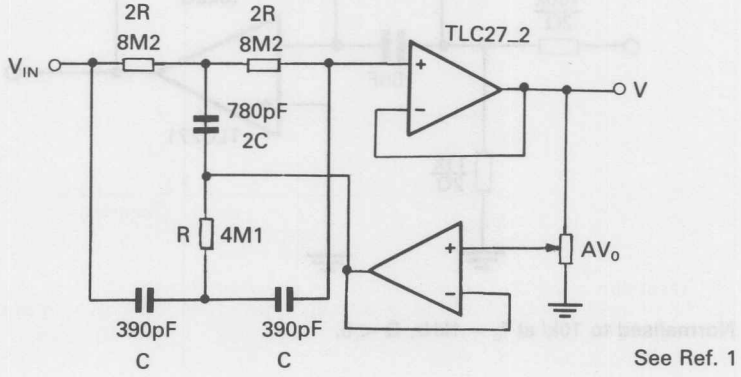


Fig. 5.33 Adjustable Q notch filter.



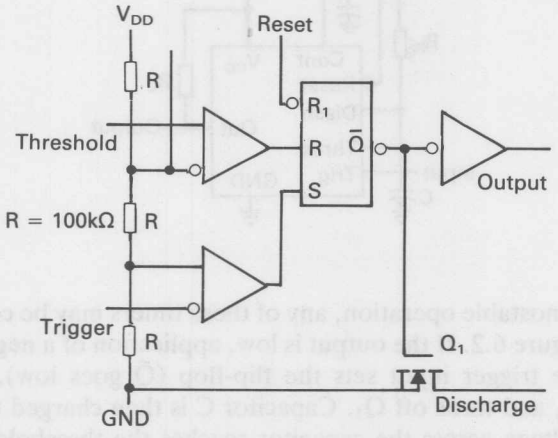
$$\frac{V_o}{V_{IN}} = \frac{4s^2R^2C^2 + 1}{4s^2R^2C^2 + (1 - A)\,8sRC + 1}$$

6. LinCMOS Timers

DESCRIPTION

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS process. Due to its high-impedance inputs (typically $10^{12}\Omega$), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors than the NE555. Like the NE555, the TLC555 achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The LinCMOS process allows the TLC555 to operate at frequencies up to 2MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 1 mW at V_{DD} = 5 V) over a wide range of supply voltages ranging from 2 volts to 18 volts.

Fig. 6.1 Functional block diagram.



1. Reset can override Trigger, which can override Threshold.
2. All unused inputs should be tied to an appropriate logic level to prevent false triggering.

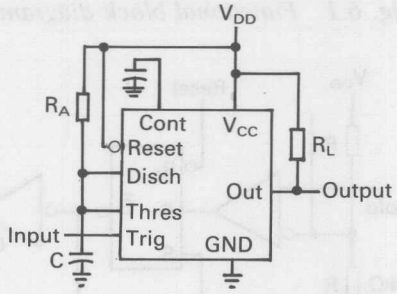
Like the NE555, the threshold and trigger levels are normally two-thirds and one-third respectively of V_{DD}. These levels can be

altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

MONOSTABLE OPERATION

Fig. 6.2 Circuit for monostable operation.



For monostable operation, any of these timers may be connected as shown in Figure 6.2. If the output is low, application of a negative-going pulse to the trigger input sets the flip-flop ($\bar{Q}$ goes low), drives the output high, and turns off Q_1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold input. If the trigger input has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\bar{Q}$ goes high), drive the output low, and discharge C through Q_1.

Monostable operation is initiated when the trigger input voltage falls below the trigger threshold. Once initiated, the sequence will

complete only if the trigger input is high at the end of the timing interval. Because of the threshold level and on-state voltage of Q_1, the output pulse duration is approximately $t_w = 1.1\ R_AC$. Figure 6.4 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{DD}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Fig. 6.3 Typical monostable waveforms.

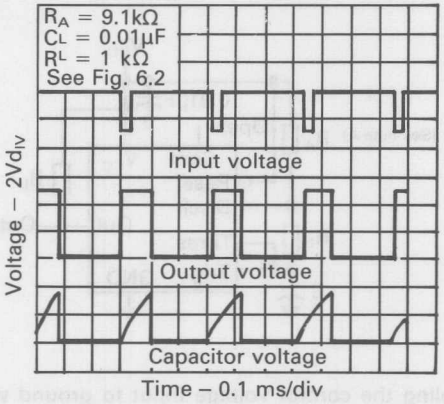
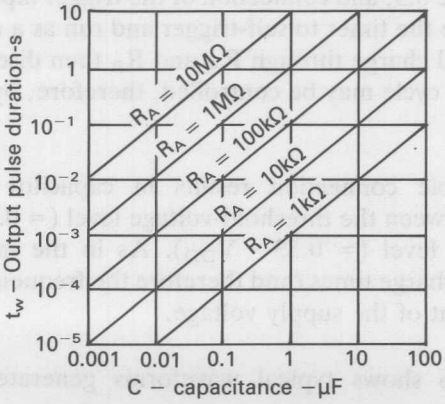


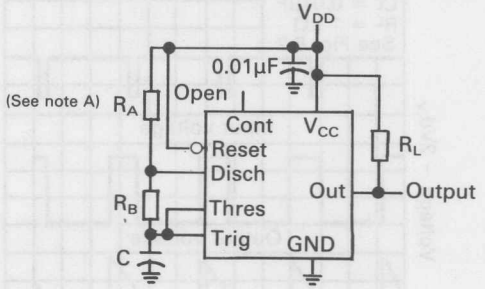
Fig. 6.4 Output pulse duration Vs. capacitance.



Applying a negative-going trigger pulse simultaneously to the reset and trigger terminals during the timing interval will discharge C and re-initiate the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. When the reset input is not used, it should be connected to V_{DD} to prevent false triggering.

ASTABLE OPERATION

Fig. 6.5 Circuit for astable operation.



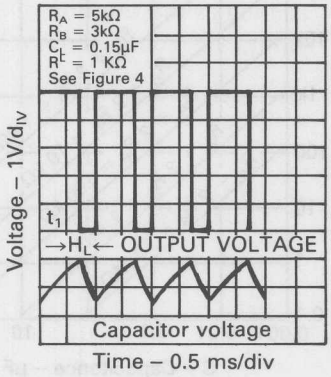
NOTE A: Decoupling the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

Addition of a second resistor, R_B, to the circuit of Figure 6.2 as shown in Figure 6.5, and connection of the trigger input to the threshold input will cause the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($= 0.67 \cdot V_{DD}$) and the trigger-voltage level ($= 0.33 \cdot V_{DD}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 6.6 shows typical waveforms generated during astable

Fig. 6.6 Typical astable waveforms.



operation. The output high-level duration t_H and low-level duration t_L may be found by:

$$t_H = 0.693\ (R_A + R_B)C$$

$$t_L = 0.693\ (R_B)C$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)C$$

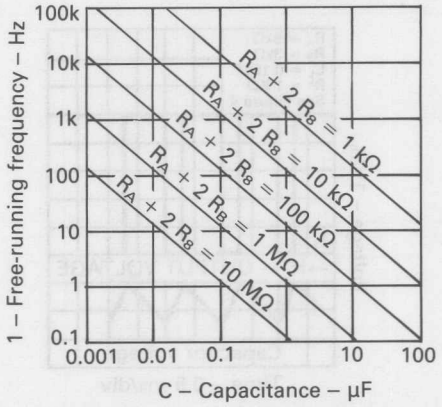
$$\text{frequency} = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

Fig. 6.7 Free-running frequency.



At astable operating frequencies above one megahertz, the propagation delays of the TLC555 must be accounted for in the equations for calculating the stable frequency. The 'ON' resistance of the NMOS discharge transistor (typically 10 ohms) is also included to give greater accuracy. Besides the low to high and high to low propagation delays, (T_{dLH} and T_{dHL} respectively), two additional times, T_c and T_d, must also be included along with the maximum charge and minimum discharge voltages, (V_h and V_i respectively).

As the capacitor is charging, as shown in Figure 6.8, it continues to charge up to V_h after crossing the 2/3 V_{DD} level for a time equal to the T_{dHL} propagation delay. T_d is the length of time it takes to discharge from V_h to 2/3 V_{DD}.

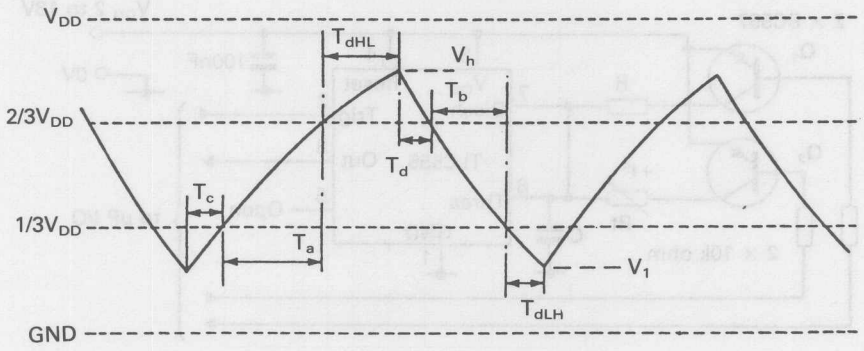
Likewise, during the discharge part of the cycle the capacitor continues to discharge down to V_i after crossing the 1/3 V_{DD} level for a time equal to T_{dLH}. T_c is the length of time required to charge back up from V_i to 1/3 V_{DD}.

$R_t = R_a + R_b \qquad R_t' = R_b + R_{don} \qquad Ln = \text{natural log}$

$T_a = 0.693R_tC_t \qquad T_b = 0.693R_t'C_t$

$V_1 = (2/3)V_{DD}EXP(-(0.693 + T_{dLH}/(R_t'C_t)))$

Fig. 6.8 Timing diagram showing propagation delays



$$V_h = (2/3)V_{DD}(1-EXP(-(0.693 + T_{dHL}/R_iC_i))) + (1/3)V_{DD}$$

$$T_c = -R_tC_tLn(1-((1/3)V_{DD} - V_1)/(V_{DD} - V_1))$$

$$T_d = -R_t'C_tLn((2/3)V_{DD}-V_h)$$

$$T_{period} = T_a + T_b + T_c + T_d + T_{dLH} + T_{dHL}$$

$$f\ astable = 1/t_{period}$$

Notice that for T_{dLH}, T_{dHL}, and R_{don} equal zero the above equations reduce to the standard equation as printed in the data for the NE555:

$$(NE555)\ T_{period} = T_a + T_b = 0.693\ (R_a + 2R_b)C_t$$

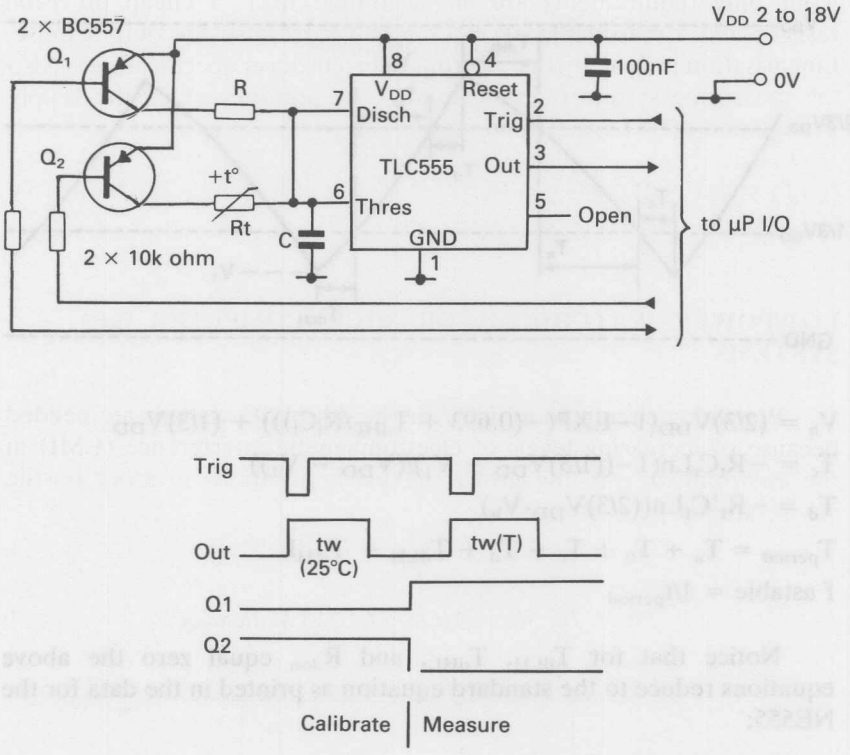
Propagation delay typical values T_{dLH} = 333nS T_{dHL} = 400nS. A 10% increase in astable frequency will also occur if an 0.1μF capacitor is connected from the control voltage pin 5 to ground.

TRANSDUCER TO μP INTERFACE USING THE TLC555

This application shows a low cost temperature sensor to μP interface, which features low sensitivity to the circuit elements and a calibration sequence.

The circuit can be generalised to other kinds of transducers, which have a variable resistance output.

Fig. 6.9 Transducer to μP interface.



Operation

R_t = PTC silicon temperature sensor, TSP102E (Texas Instruments).
R_t (25°C) = 1 kohms ± 0.5%.
R = 1 kohms ± 0.1% metal film, TC = ± 25ppm/°C.

Assume that Q_2 has been set on and Q_1 off by the μP. Then the μP sends out a trigger signal (TRIG) and receives an output pulse (OUT) with a temperature dependent duration. The temperature sensitivity is provided by the PTC termistor, R_t in the timing network.

To calibrate the system, replace R_t with the precision resistor R (Q_1 on, Q_2 off). The nominal value of R corresponds to R_t at 25°C.

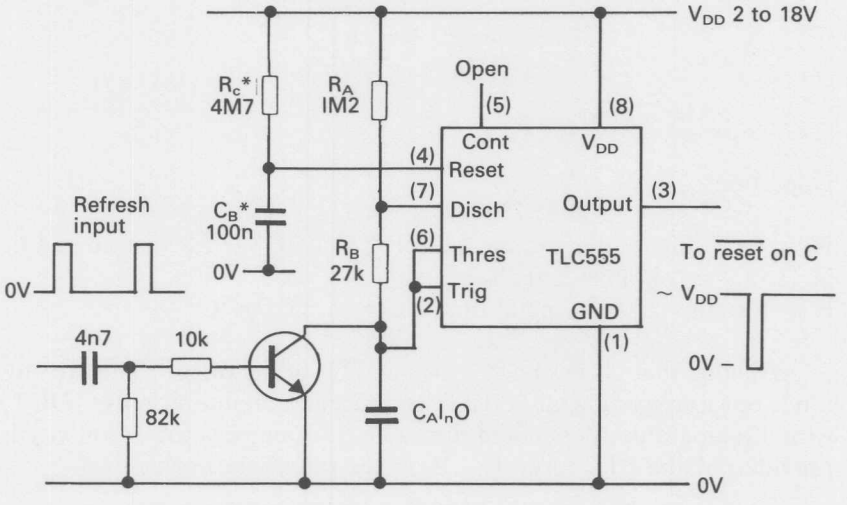
The advantage of this system is that you do not need either an accurate voltage or current, or a potentiometer for offset adjustment. Your only requirements are an accurate sensor, a cheap precision resistor and a reasonable μP clock speed to resolve the output pulse. Linearisation is done by the μP from the transducer specifications. Also the measuring system is insensitive to the accuracy of C, the supply voltage and the TLC555 timing interval errors.

t_w (T) = 1.1 × R_t × C
t_w (25°C) = 1.1 × R × C

LOWPOWER WATCHDOG FOR MICROCOMPUTER (μC) SYSTEMS

Watchdog circuits to monitor the health of μC systems are needed because of increasing levels of electromagnetic interference (EMI) in the environment and the growth of μC applications in more hostile environments.

Fig. 6.10 LinCMOS TLC555 Watchdog.



All μC systems can crash because EMI causes errors to occur within μC's at the hardware level. This is a general problem but, particularly, a protection circuit is needed for low power, low voltage battery operated CMOS systems. These requirements are met with the LinCMOS TLC555 circuit shown below with operation down to 2V (1V with TLC551) and power levels compatible with CMOS systems.

OPERATION

C_A is continually discharged by the REFRESH input to prevent the normal astable operation of the TLC555. Absence of a REFRESH input will cause an output pulse to the μC RESET. The RESET output pulse width $t_o = (0.693\ R_BC_A) = 20\mu S$ for the above circuit. A REFRESH repetition rate less than $t_i = 0.693\ (R_A + R_B)C_A = 1mS$ is required for above circuit configuration.

*R_CC_B is optionally included to delay the RESET output at power-on for use with slow start PSU's such as switch mode types. Otherwise connect reset to V_{DD}. REFRESH input is taken from a μC output port pin preferably driven from a watchdog software routine but any regularly strobed output such as display or keyboard scanning signals could be used. Power consumption at 3V V_{DD} would be typically less than 370 μW.

7. LinCMOS Comparators

INTRODUCTION

Texas Instruments has recently introduced the first commercially available CMOS comparators. The dual TLC372 and quad TLC374 are fabricated using the polysilicon-gate LinCMOS process giving the devices stable thresholds with time, temperature and applied gate-voltage. It has been previously impractical to produce CMOS comparators using the metal-gate process because of it's inherent threshold shifts with gate voltage stress, typically exceeding 10mV/V of applied gate voltage. This contrasts with the 55μV/V of the phosphorous-doped polysilicon gates of the LinCMOS process which is described in the op-amp section.

Quad comparator TLC374 is pin compatible with the industry standard LM339 but provides nearly twice the speed for half the power. Response to a 100mV step with 5mV overdrive is typically 650ns at a V_{DD} of 5V with a typical supply current of 0.4mA (100µA per comparator). Dual comparator TLC372 has the same performance and is pin compatible with the popular LM393.

USER BENEFITS

The TLC372/374's high input impedance (10^{12} ohms) and low input bias currents (10pA typical) bring the usual advantages of greater accuracy with high impedance voltage sources. For example, these sources can be high impedance transducers, voltage dividers or C–R timing circuits. Coupled with the enhanced time and temperature stability these advantages allow circuit designs with greater accuracy than has hitherto been possible with standard bipolar devices.

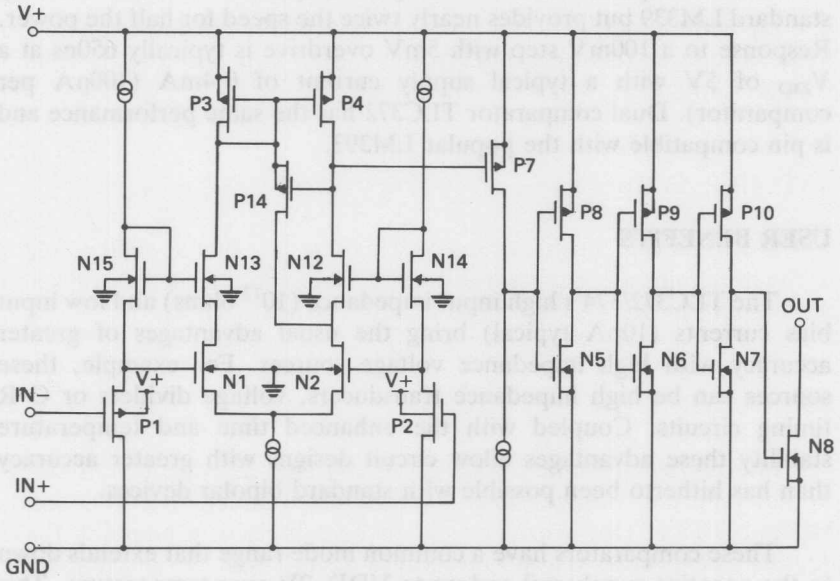
These comparators have a common mode range that extends down to the negative supply rail and up to VDD–2V over temperature. This allows operation with either single or dual supply voltages that total 2 to 18 Volts.

LinCMOS COMPARATOR CIRCUIT

A comparator is the simplest form of analogue to digital converter consisting of a differential input stage with wide common mode range and a high gain amplifying stage without compensation to slow it down. The outputs of the TLC372/374 are TTL or CMOS compatible and are in the form of a n-MOS transistor with an open drain. This allows the wired-AND function to be performed.

Figure 7.1 shows a simplified TLC372/374 comparator circuit (i.e. without biasing or ESD protection).

Fig. 7.1 LinCMOS TLC37_ comparator simplified schematic (i.e. without ESD or Bias Circuitry).



Having an input range to GND, p-MOS transistors P_1,P_2 act as source followers feeding differential amplifier N_1,N_2 which in turn drives P_3,P_4 differential to single-ended converter. The output from this circuit drives a buffer consisting of P_7 and complementary pairs P_8,N_5,

P_9,N_6 and P_{10},N_7 to give comparator output from N_8 drain. Stages $N_{13/15}$, $N_{12/14}$ and P_{14} clamp circuit voltages to speed operation by preventing charging and discharging of circuit capacitances.

TESTING

Testing or operating these comparators in a linear mode is not possible because of the complementary nature of the buffer. This would require that the output is held in the middle of the transition region with both n-MOS and p-MOS devices "ON" simultaneously causing excessive supply current, I_{DD}, to flow. A binary search method has to be used to measure offset voltage.

OUTPUT VOLTAGE RANGE

Open drain output voltage can be taken above the device operating V_{DD} as long as this does not exceed the 18 volt absolute maximum voltage rating.

LATCHUP AVOIDANCE

Latchup avoidance is achieved by making sure that applied voltages to the input pins are not greater than 0.3 V beyond the supply rails and the output pin does not go more than 0.3 V below GND.

ESD PROTECTION

Internal electrostatic discharge (ESD) circuits will prevent catastrophic failure at voltages up to 2 kV as tested under MIL-STD-883B, Method 3015.1. However care should be exercised in handling these devices as exposure to ESD may cause degradation of the parametric performance.

REFERENCES

1. The Bifet Design Manual 1984/85. Peter F. Nicholson & Stuart Miller. Texas Instruments.

2. Reference Data for Radio Engineers. ITT. Howard W. Sams & Co.

3. Active Filter Cookbook. Don Lancaster. Howard W. Sams & Co. 1975.

4. Electronic Filter Design Handbook. Arthur B. Williams. McGraw-Hill Book Company. 1981.

5. Introduction to the Theory and design of Active Filters. L. P. Huelsman and P. E. Allen. McGraw-Hill Book Company. 1980.

6. Operation Amplifiers Design and Applications. Tobey-Graeme-Huelsman. McGraw-Hill Book Company 1981.

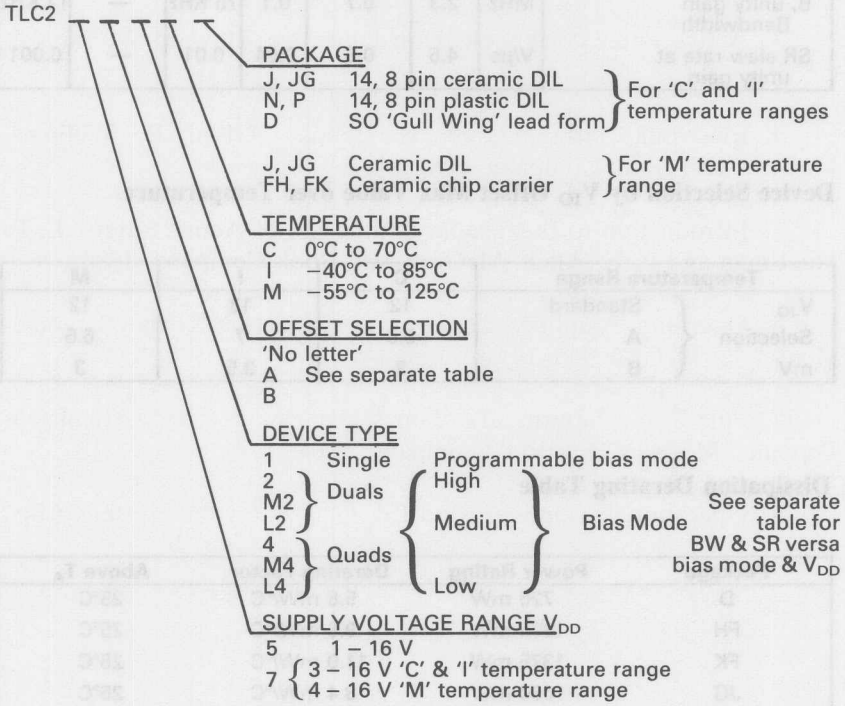
7. Pole-Zero Patterns. E. James Angelo, Jr. and Athanasios Papoulis. McGraw-Hill Book Company. 1964.

8. Operational Amplifiers 2nd Ed. G. B. Clayton. Butterworths. 1979.

8. Data Sheets

LinCMOS OP-AMP SELECTION

Build a Device Number



e.g. (1) TLC25L4ACD is a low bias mode Quad in SO package with V_{IO} selection of 6.5 mV and 'C' temperature range.

(2) TLC271CP is a 3–16V single of 'C' temperature range in 8 pin plastic DIL package.

Device Selection by Bias Mode

Device Type		TLC 27X/25X			TLC25X		
V_{DD} supply voltage	V	10			1		
Bias mode		High	Medium	Low	High	Medium	Low
I_{DD} supply current (each amp)	μA	1000	150	10	12	—	2
B, unity gain Bandwidth	MHz	2.3	0.7	0.1	75 KHz	—	12 KHz
SR slew rate at unity gain	V/μs	4.5	0.6	0.04	0.01	—	0.001

Device Selection by V_{IO} Offset Max Value over Temperature

Temperature Range		C	I	M
V_{JO} Selection mV	Standard	12	13	12
	A	6.5	7	6.5
	B	3	3.5	3

Dissipation Derating Table

Package	Power Rating	Derating Factor	Above T_A
D	725 mW	5.8 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11.0 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

Interchangeability Suggestion

LinCMOS op-amps, by type and bias mode, may be interchangeable with the devices shown in the chart for particular applications. The LinCMOS types should be considered for replacing these types in existing or new designs.

Singles TLC271 (UA741 type pinout)		**Duals TLC27–2 (Pin compatible)**		**Quads TLC27–4 (Pin compatible)**	
Device	Suggested bias mode	Device	Suggested bias mode	Device	Suggested bias mode
CA3140	H	CA3240	H	ICL764X	ALL
CA3160	H	CA3260	H	LF347	H
CA3440	L	ICL762X	ALL	LF444	M
ICL761X	ALL	LF353	H	LM324	M
LF13741	M	LF412	H	LM326	ALL
LF351	H	LF442	M	LM348	M
LF356	H	LM358	M	MC4741C	M
LF411	H	MC1458	M	TLO64	M
LF441	M	MC3458	M	TLO74/84	H
LM301A	M	RC4558	H		
MC3476	ALL	TLO22	M		
TLO61	M	TLO62	M		
TLO71/81	H	TLO72/82	H		
TL321	M				
UA741	M				

TLC2__ 'L' bias modes' lower slew rate and bandwidth may not be a disadvantage in d.c. and instrumentation applications, but will give a low power advantage when substituted for devices in the chart.

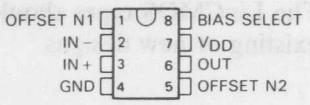
LINEAR INTEGRATED CIRCUITS

TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B PROGRAMMABLE LOW-POWER LinCMOS™ OPERATIONAL AMPLIFIERS

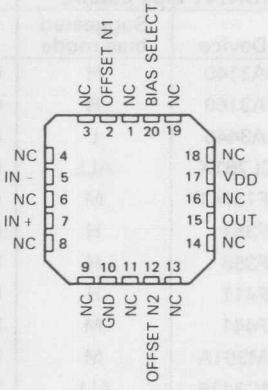
D2751, JULY 1983 – REVISED NOVEMBER 1983

- **Wide Range of Supply Voltages:**
  1 V to 16 V (TLC251C)
  3 V to 16 V (TLC271C, TLC271I)
  4 V to 16 V (TLC271M)
- **True Single Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV/$\sqrt{Hz}$ Typ at 1 kHz (High Bias)**

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



FH OR FK PACKAGE
(TOP VIEW)

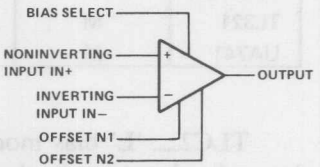


NC No internal connection

description

The TLC251 and TLC271 series are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The TLC251 offers the same operation sd the TLC271, but also features guaranteed operation down to a 1 V supply. Both devices are stable at unity gain.

symbol



TEMPERATURE RANGES AND PACKAGES

SERIES	TEMPERATURE RANGE	PACKAGES
TLC251_C Types	0°C to 70°	JG, P, D
TLC271_C Types	0°C to 70°C	JG, P, D
TLC271_I Types	–40°C to 85°C	JG, P, D
TLC271_M Types	–55°C to 125°C	JG, FH, FK

DEVICE FEATURES

PARAMETER	LOW BIAS	MEDIUM BIAS	HIGH BIAS
Supply current (Typ)	10 μA	150 μA	1000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
. . . Standard types	10 mV	10 mV	10 mV
. . . A-suffix types	5 mV	5 mV	5 mV
. . . B-suffix types	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

†The long-term drift value applies after the first month.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS

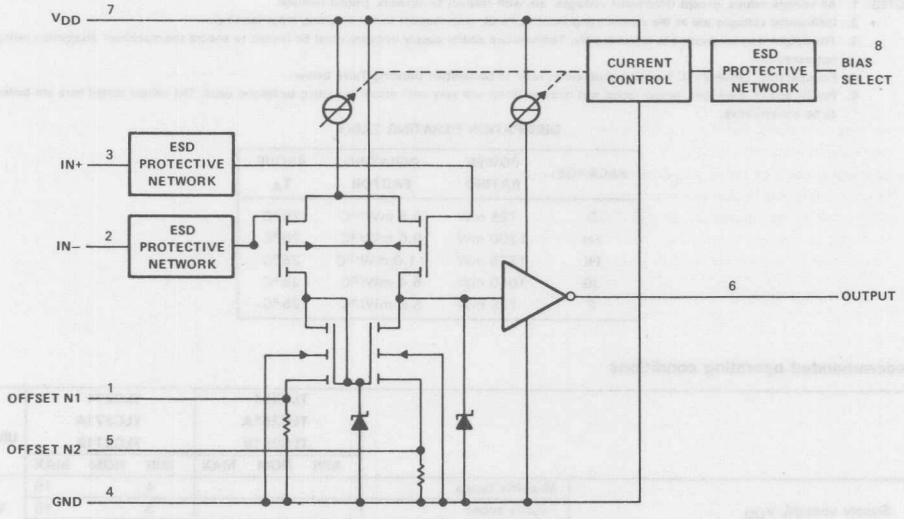
TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B PROGRAMMABLE LOW-POWER LinCMOS™ AMPLIFIERS

description (continued)

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251 and TLC271 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251 is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications.

schematic



TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B PROGRAMMABLE LOW-POWER LinCMOS™ AMPLIFIERS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4):
D package . . . . . 725 mW
FH package (see Note 5) . . . . . 1200 mW
FK package (see Note 5) . . . . . 1375 mW
JG package . . . . . 1050 mW
P package . . . . . 725 mW
Operating free-air temperature range: TLC271M, TLC271AM, TLC271BM . . . . . −55°C to 125°C
TLC271I, TLC271AI, TLC271BI . . . . . −40°C to 85°C
TLC251C, TLC251AC, TLC251BC,
TLC271C, TLC271AC, TLC271BC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . . 300°C
Lead Temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Table below.
5. For FH and FK packages, power rating and rerating factor will vary with actual mounting technique used. The values stated here are believed to be conservative.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11.0 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

recommended operating conditions

		TLC251 TLC251A TLC251B			TLC271 TLC271A TLC271B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	M-suffix types				4		16	V
	I-suffix types				3		16	
	C-suffix types	1		16	3		16	
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	−0.2		0.2				V
	V_{DD} = 4 V	−0.2		3	−0.2		3	
	V_{DD} = 10 V	−0.2		9	−0.2		9	
	V_{DD} = 16 V	−0.2		14	−0.2		14	
Operating free-air temperature, T_A	M-suffix types				−55		125	°C
	I-suffix types				−40		85	
	C-suffix types	0		70	0		70	
Bias Select pin voltage		See application notes						

TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B PROGRAMMABLE LOW-POWER LinCMOS™ AMPLIFIERS

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		BIAS	TLC271_M			TLC271_I			TLC251_C, TLC271_C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251_, TLC271_	V_O = 1.4 V, R_S = 50 Ω	25°C	Any			10			10			10	mV
				Full range				12			13			12	
		TLC251A_, TLC271A_		25°C	Any			5			5			5	
				Full range				6.5			7			6.5	
		TLC251B_, TLC271B_		25°C	Any			2			2			2	
				Full range				3			3.5			3	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range	Low		0.7			0.7			0.7		μV/°C
					Medium		2			2			2		
					High		5			5			5		
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1			1			1		pA
				Full range				15000			1000			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1			1			1		pA
				Full range				35000			2000			600	
V_{ICR}	Common-mode input voltage range			25°C	Any	-0.2 to 9			-0.2 to 9			-0.2 to 9			V
V_{OM}	Peak output voltage range‡		V_{ID} = 100 mV	25°C	Any	8	8.6		8	8.6		8	8.6		V
				Full range		7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	Low	30	500		30	500		30	500		V/mV
					Medium	20	280		20	280		20	280		
					High	10	40		10	40		10	40		
				Full range	Low	20			20			25			
					Medium	10			10			15			
					High	7			7			7.5			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	Any	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	Low	70	88		70	88		70	88		dB
					Medium	70	88		70	88		70	88		
					High	65	82		65	82		65	82		
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C	Any		-55			-55			-55		mA
			V_O = V_{DD}, V_{ID} = -100 mV				15			15			15		
$I_{IH(SEL)}$	High-level input current to bias select		$V_{I(SEL)}$ = 0 V	25°C	High		10.5			10.5			10.5		μA
$I_{IL(SEL)}$	Low-level input current to bias select		$V_{I(SEL)}$ = 10 V	25°C	Low		1.3			1.3			1.3		μA
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C	Low		10	20		10	20		10	20	μA
					Medium		150	300		150	300		150	300	
					High		1000	2000		1000	2000		1000	2000	
				Full range	Low			40			40			30	
					Medium			500			500			400	
					High			3000			2500			2200	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for TLC2__M, −40°C to 85°C for TLC2__I, and 0°C to 70°C for TLC2__C. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER			TEST CONDITIONS†		BIAS	TLC251_C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average Temperature Coefficient of Input Offset Voltage			0°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				100	
I_{IB}	Input bias current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				150	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	Any		450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, V_{IC} = V_{IC} min	25°C	Any		77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C	Low		2		μA
					High		12		

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	TLC251_C			UNIT
				MIN	TYP	MAX	
B_1	Unity-gain bandwidth	C_L = 10 pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B PROGRAMMABLE LOW-POWER LinCMOS™ AMPLIFIERS

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	TLC2_M			TLC2_I			TLC2_C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50Ω	Low		0.1			0.1			0.1		MHz
			Medium		0.7			0.7			0.7		
			High		2.3			2.3			2.3		
SR	Slew rate at unity gain	See Figure 1	Low		0.04			0.04			0.04		V/μs
			Medium		0.6			0.6			0.6		
			High		4.5			4.5			4.5		
	Overshoot factor	See Figure 1	Low		30%			30%			30%		
			Medium		35%			35%			35%		
			High		35%			35%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = pF	Low		43°			43°			43°		
			Medium		43°			43°			43°		
			High		50°			50°			50°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	Low		70			70			70		nV/√Hz
			Medium		38			38			38		
			High		30			30			30		

PARAMETER MEASUREMENT INFORMATION

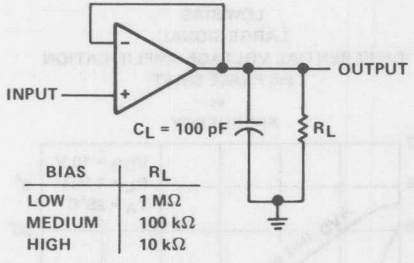


FIGURE 1–UNITY-GAIN AMPLIFIER

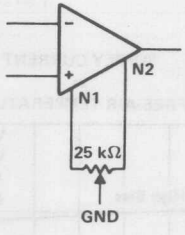


FIGURE 2–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

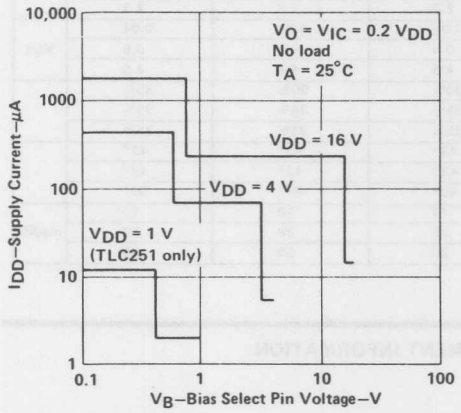
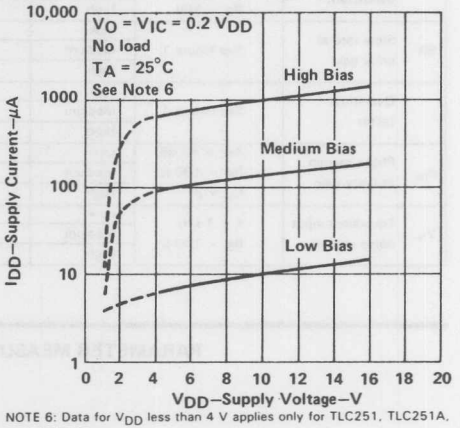


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE



NOTE 6: Data for V_{DD} less than 4 V applies only for TLC251, TLC251A, and TLC251B.

FIGURE 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

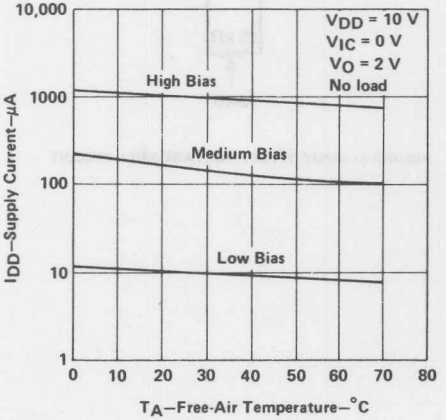


FIGURE 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

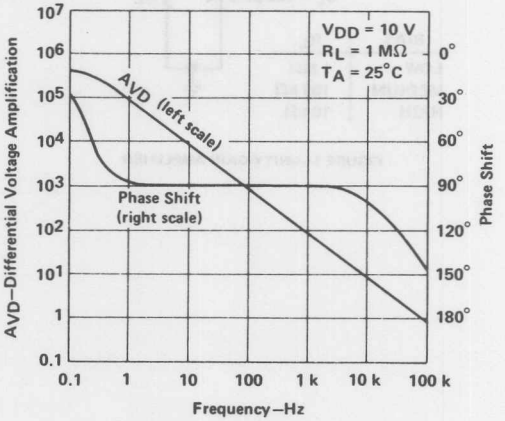


FIGURE 6

TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B
PROGRAMMABLE LOW-POWER LinCMOS™ AMPLIFIERS

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

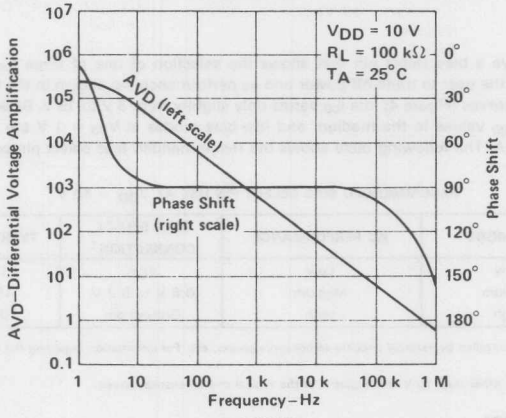


FIGURE 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

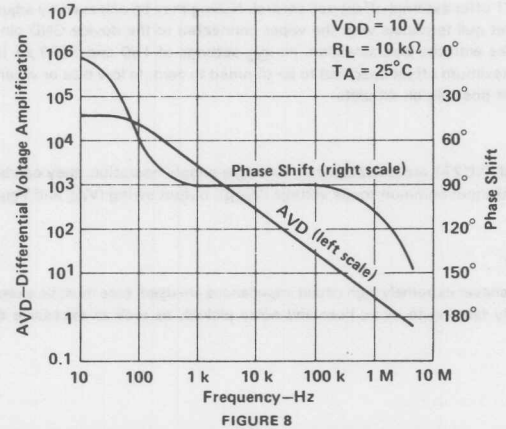


FIGURE 8

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251 and TLC271 have a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 3 V to 16 V. Below 3 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V:

RECOMMENDED BIAS SELECT PIN USE AT V_{DD} = 10 V

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}§
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

†The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.

§For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

input offset nulling

Both the TLC251 and TLC271 offer external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At I_{DD} settings of 150 and 1000 μA (medium and high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low bias or when the TLC251 is used below 4 V, total nulling may not be possible on all units.

supply configurations

Even though the TLC251 and TLC271 are characterized for single-supply operation, they can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

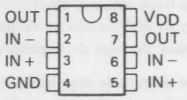
LINEAR INTEGRATED CIRCUITS

TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2 LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

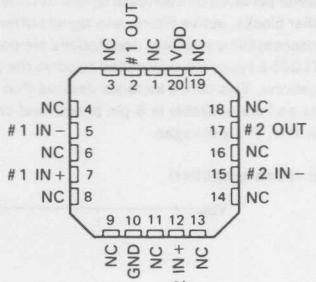
D2752, JUNE 1983–REVISED OCTOBER 1983

- **Wide Range of Supply Voltages:**
  1 V to 16 V (TLC252C)
  3 V to 16 V (TLC272C, TLC272I)
  4 V to 16 V (TLC272M)
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)**

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



FH OR FK PACKAGE
(TOP VIEW)

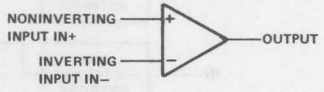


NC–No internal connection

description

The TLC252 and TLC272 series are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The TLC252 types offer guaranteed operation down to a 1-V supply. All devices are unity-gain stable and have excellent noise characteristics.

symbol (each amplifier)



DEVICE FEATURES

PARAMETER	TLC25L2 TLC27L2 (LOW BIAS)	TLC25M2 TLC27M2 (MEDIUM BIAS)	TLC252 TLC272 (HIGH BIAS)
Supply current (Typ)	20 μA	300 μA	2000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
. . . Standard types	10 mV	10 mV	10 mV
. . . A-suffix types	5 mV	5 mV	5 mV
. . . B-suffix types	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

†The offset voltage drift applies after the first month only.

TEMPERATURE RANGES AND PACKAGES

TYPES	TEMPERATURE RANGE	PACKAGES
TLC25_2_C	0°C to 70°	JG, P, D
TLC27_2_C	0°C to 70°C	JG, P, D
TLC27_2_I	–40°C to 85°C	JG, P, D
TLC27_2_M	–55°C to 125°C	JG, FH, FK

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS

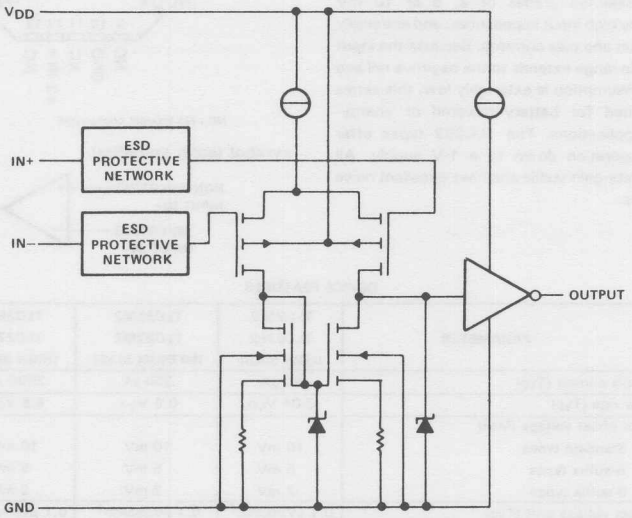
TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL APPLIFIERS

description (continued)

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252 and TLC272 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252 and TLC272 series. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC252. The TLC252 types are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for commercial, industrial, and military temperature ranges and are available in 8-pin plastic and ceramic dual-in-line (DIP) packages, small outline (D) package, and chip carrier (FH, FK) packages.

schematic (each amplifier)



TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2 LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4):
D package . . . . . 725 mW
FH package (see Note 5) . . . . . 1200 mW
FK package (see Note 5) . . . . . 1375 mW
JG package . . . . . 1050 mW
P package . . . . . 725 mW
Operating free-air temperature range: TLC27_2_M . . . . . −55°C to 125°C
TLC27_2_I . . . . . −40°C to 85°C
TLC25_2_C, TLC27_2_C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.
5. For FH and FK packages, power rating and derating factor will vary with the actual mounting technique used. The values stated here are believed to be conservative.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

recommended operating conditions

		TLC25_2 TLC25_2A TLC25_2B			TLC27_2 TLC27_2A TLC27_2B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	M-suffix types				4		16	V
	I-suffix types				3		16	
	C-suffix types	1		16	3		16	
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	−0.2		0.2				V
	V_{DD} = 4 V	−0.2		3	−0.2		3	
	V_{DD} = 10 V	−0.2		9	−0.2		9	
	V_{DD} = 16 V	−0.2		14	−0.2		14	
Operating free-air temperature, T_A	M-suffix types				−55		125	°C
	I-suffix types				−40		85	
	C-suffix types	0		70	0		70	

TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C, TLC272_C			TLC25L2_C, TLC27L2_C			TLC25M2_C, TLC27M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC2_2C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC2_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC2_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0° to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2200			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 1 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current (each amplifier)		No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-ggin bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

TYPES TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

M-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC272_M			TLC27L2_M			TLC27M2_M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_2M	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				−55°C to 125°C			12			12			12	
		TLC27_2AM		25°C			5			5			5	
				−55°C to 125°C			6.5			6.5			6.5	
		TLC27_2BM		25°C			2			2			2	
				−55°C to 125°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			−55°C to 125°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			15			15			15	nA
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			35			35			35	nA
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				−55°C to 125°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				−55° to 125°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				−55°C to 125°C			3000			40			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

TYPES TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

I-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC272_I			TLC27L2_I			TLC27M2_I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_2I	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				−40°C to 85°C			13			13			13	
		TLC27_2AI		25°C			5			5			5	
				−40°C to 85°C			7			7			7	
		TLC27_2BI		25°C			2			2			2	
				−40°C to 85°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			−40°C to 85°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−40°C to 85°C			1000			1000			1000	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−40°C to 85°C			2000			2000			2000	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				−40°C to 85°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				−40°C to 85°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR}min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				−40°C to 85°C			2500			40			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C TLC272_M TLC272_I TLC272_C			TLC25L2_C TLC27L2_M TLC27L2_I TLC27L2_C			TLC25M2_C TLC27M2_M TLC27M2_I TLC27M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		nV/√Hz
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

PARAMETER MEASUREMENT INFORMATION

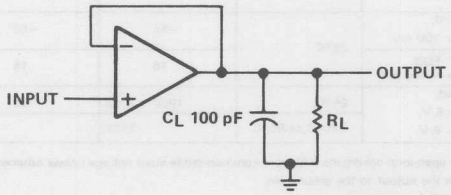


FIGURE 1–UNITY GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

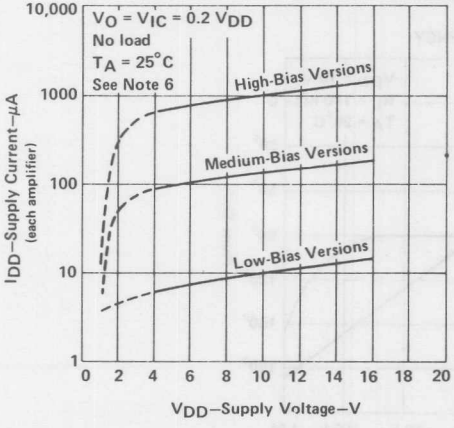


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

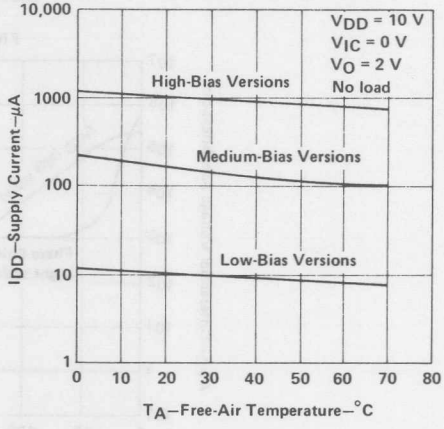


FIGURE 3

NOTE 6: Data for V_{DD} less than 4 V does not apply for the TLC272 series.

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

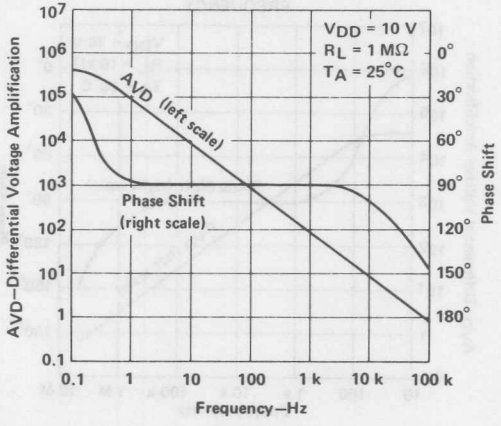


FIGURE 4

TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

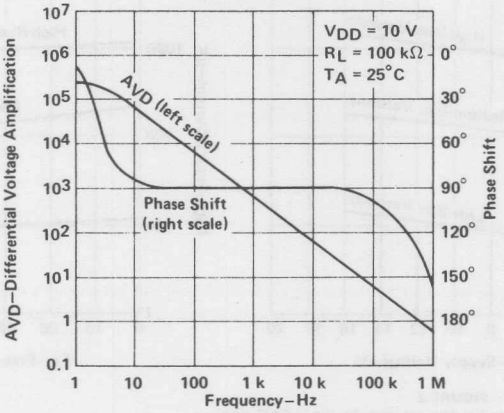


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

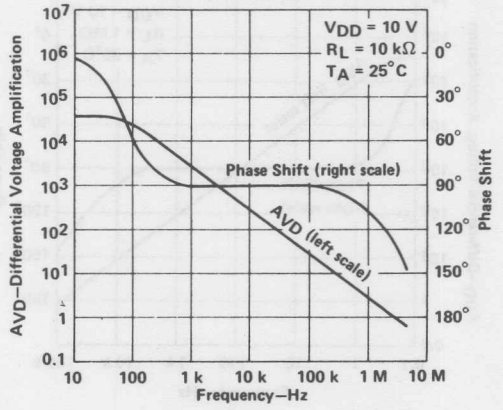


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, any input signals are applied.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC252 and TLC272 are characterized for single-supply operation, they can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

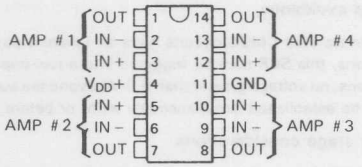
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

TYPES TLC254, TLC25L4, TLC25M4, TLC274, TLC27L4, TLC27M4
LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

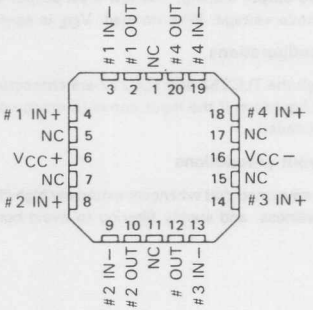
D2753, JUNE 1983 – REVISED NOVEMBER 1983

- **Wide Range of Supply Voltages:**
  1 V to 16 V (TLC254C)
  3 V to 16 V (TLC274C, TLC274I)
  4 V to 16 V (TLC274M)
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)**

D, J, OR N DUAL IN-LINE-PACKAGE
(TOP VIEW)



FH OR FK PACKAGE
(TOP VIEW)

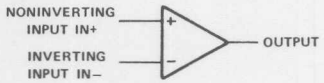


NC – No internal connection

description

The TLC254 and TLC274 series are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The TLC254 types offer guaranteed operation down to a 1-V supply. All devices are unity-gain stable and have excellent noise characteristics.

symbol (each amplifier)



TEMPERATURE RANGES AND PACKAGES

TYPES	TEMPERATURE RANGE	PACKAGES
TLC25_4_C	0°C to 70°	J, N, D
TLC27_4_C	0°C to 70°C	J, N, D
TLC27_4_I	–40°C to 85°C	J, N, D
TLC27_4_M	–55°C to 125°C	J, FH, FK

DEVICE FEATURES

PARAMETER	TLC25L4 TLC27L4 (LOW BIAS)	TLC25M4 TLC27M4 (MEDIUM BIAS)	TLC254 TLC274 (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
. . . Standard types	10 mV	10 mV	10 mV
. . . A-suffix types	5 mV	5 mV	5 mV
. . . B-suffix types	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

†The long-term drift value applies after the first month.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS

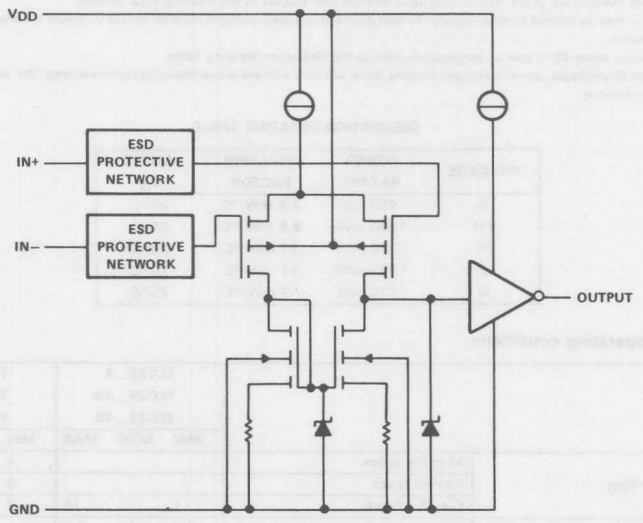
TYPES TLC254, TLC25L4, TLC25M4, TLC274, TLC27L4, TLC27M4 LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

description (continued)

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254 and TLC274 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC254 and TLC274 series. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC254. The TLC254 types are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for commercial, industrial, and military temperature ranges and are available in 14-pin plastic and ceramic dual-in-line (DIP) packages, small outline (D) package, and chip carrier (FH, FK) packages.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4):
D package . . . . . 950 mW
FH package (see Note 5) . . . . . 1200 mW
FK package (see Note 5) . . . . . 1375 mW
J package . . . . . 1375 mW
N package . . . . . 875 mW
Operating free-air temperature range: TLC27_4_M . . . . . −55°C to 125°C
TLC27_4_I . . . . . −25°C to 85°C
TLC25_4_C, TLC27_4_C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.
5. For FH and FK packages, power rating and derating factor will vary with the actual mounting technique used. The values stated hee are belived to be conservative.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
J	1375 mW	11 mW/°C	25°C
N	875 mW	7 mW/°C	25°C

recommended operating conditions

		TLC25_4 TLC25_4A TLC25_4B			TLC27_4 TLC27_4A TLC27_4B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	M-suffix types				4		16	V
	I-suffix types				3		16	
	C-suffix types	1		16	3		16	
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	−0.2		0.2				V
	V_{DD} = 4 V	−0.2		3	−0.2		3	
	V_{DD} = 10 V	−0.2		9	−0.2		9	
	V_{DD} = 16 V	−0.2		14	−0.2		14	
Operating free-air temperature, T_A	M-suffix types				−55		125	°C
	I-suffix types				−40		85	
	C-suffix types	0		70	0		70	

TYPES TLC274, TLC27L4, TLC27M4
LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

M-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC274_M			TLC27L4_M			TLC27M4_M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_4M	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				−55°C to 125°C			12			12			12	
		TLC27_4AM		25°C			5			5			5	
				−55°C to 125°C			6.5			6.5			6.5	
		TLC27_4BM		25°C			2			2			2	
				−55°C to 125°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			−55°C to 125°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			15			15			15	nA
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			35			35			35	nA
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				−55°C to 125°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				−55° to 125°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				−55°C to 125°C			3000			40			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

I-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC274_I			TLC27L4_I			TLC27M4_I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_4I	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				−40°C to 85°C			13			13			13	
		TLC27_4AI		25°C			5			5			5	
				−40°C to 85°C			7			7			7	
		TLC27_4BI		25°C			2			2			2	
				−40°C to 85°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			−40°C to 85°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−40°C to 85°C			1000			1000			1000	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−40°C to 85°C			2000			2000			300	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				−40°C to 85°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				−40°C to 85°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				−40°C to 85°C			2500			40			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

TYPES TLC254, TLC25L4, TLC25M4, TLC274, TLC27L4, TLC27M4
LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C, TLC274_C			TLC25L4_C, TLC27L4_C			TLC25M4_C, TLC27M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC2_4C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC2_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC2_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0° to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2200			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 1 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current (each amplifier)		No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

TYPES TLC254, TLC25L4, TLC25M4, TLC274, TLC27L4, TLC27M4 LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C TLC274_M TLC274_I TLC274_C			TLC25L4_C TLC27L4_M TLC27L4_I TLC27L4_C			TLC25M4_C TLC27M4_M TLC27M4_I TLC27M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MH_z
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross talk attenuation	A_V = 100		120			120			120		dB

PARAMETER MEASUREMENT INFORMATION

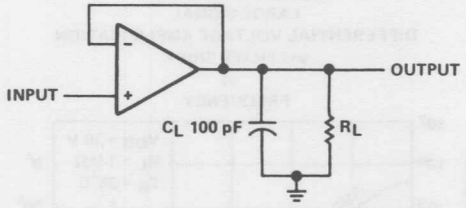


FIGURE 1–UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

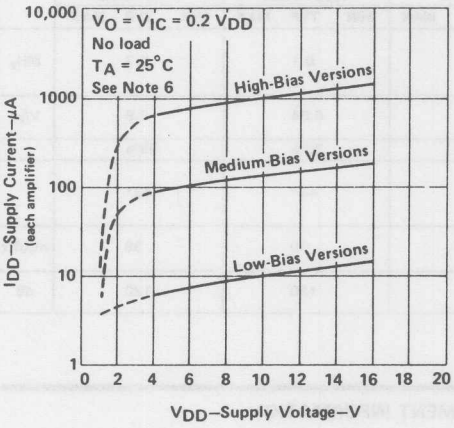


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

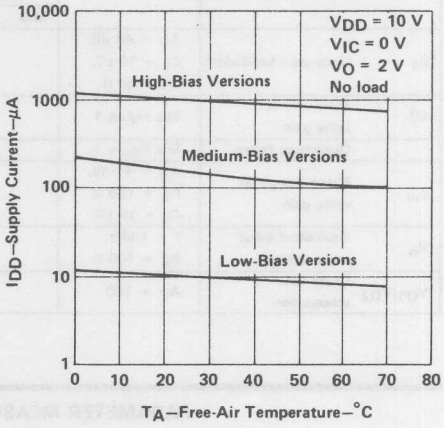


FIGURE 3

NOTE 6: Data for V_{DD} less than 4 V does not apply for the TLC274 series.

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

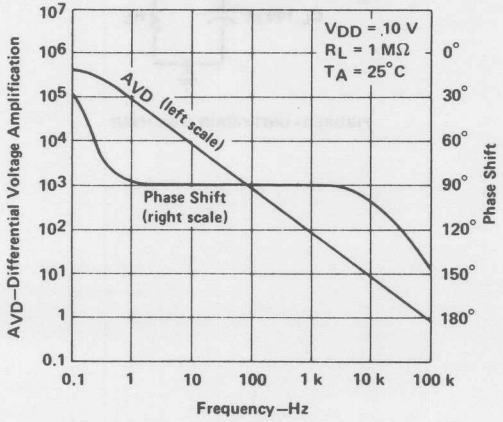


FIGURE 4

TYPES TLC254, TLC25L4, TLC25M4, TLC274, TLC27L4, TLC27M4
LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

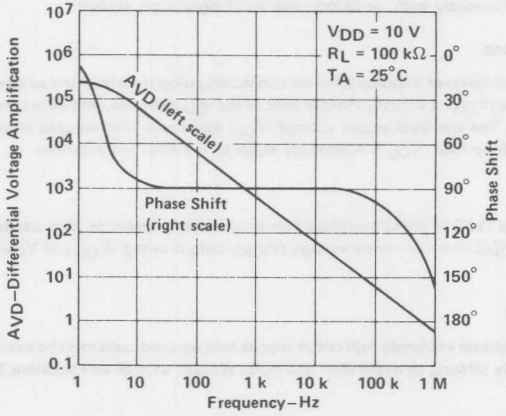


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

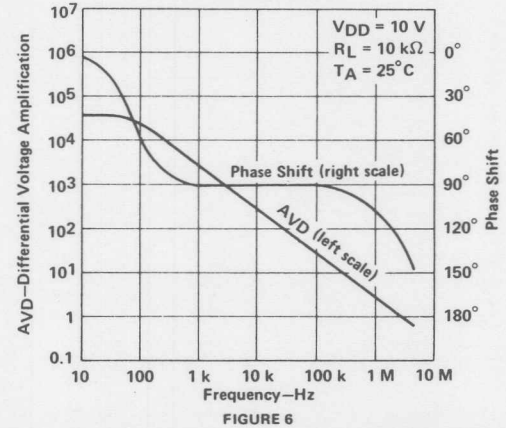


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, any input signals are applied.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC254 and TLC274 are characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

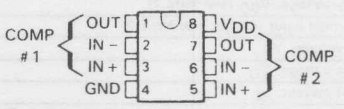
LINEAR INTEGRATED CIRCUITS

TYPES TLC372M, TLC372C
DUAL LinCMOS™ DIFFERENTIAL COMPARATORS

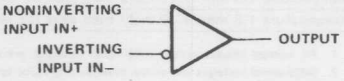
D2821, NOVEMBER 1983

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages 2 to 18 Volts
- Very Low Supply Current Drain 0.2 mA Typ
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Ω Typ
- Extremely Low Input Bias Current 1 pA Typ
- Ultra-Stable Low Input Offset Voltage
- Common-Mode Input Voltage Range Includes Ground
- Output Compatible with TTL, MOS, and CMOS

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each of these devices features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372C is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

TYPES TLC372M, TLC372C
DUAL LinCMOS™ DIFFERENTIAL COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC374M	TLC374C	UNIT
Supply voltage, V_{DD} (see Note 1)		18	18	V
Differential input voltage (see Note 2)		±18	±18	V
Input voltage, V_I		18	18	V
Output voltage, V_O		18	18	V
Output current, I_O		20	20	mA
Duration of output short-circuit to ground (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, TLC374C chips are glass mounted and TLC374M chips are alloy mounted.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC372M			TLC372C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 5		25°C		2	10		2	10	mV
				Full range			12			12	
I_{IO}	Input offset current	See Note 5		25°C		1			1		pA
				Full range			10			0.3	nA
I_{IB}	Input bias current			25°C		1					pA
				Full range			20			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} −1.5			0 to V_{DD} − 1.5			V
				Full range	0 to V_{DD} − 2			0 to V_{DD} − 2			
A_{VD}	Large-signal differential voltage amplification	V_{DD} = 15 V, R_L ≥ 15 kΩ to V_{DD}		25°C		200			200		v/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} 4 mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		0.2			0.2		mA

†All characteristics are measured with zero common-mode input voltage unless otherwise specified.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output up to 4 V or down to 400 mV with a pull-up resistor of 2.5 kΩ to V_{DD}. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance. Full range for T_A is −55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

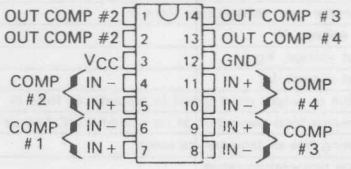
LINEAR INTEGRATED CIRCUITS

TYPES TLC374M, TLC374C QUADRUPLE LinCMOS™ DIFFERENTIAL COMPARATORS

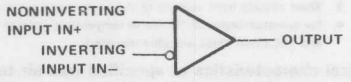
D2783 NOVEMBER 1983

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages 2 to 18 volts
- Very Low Supply Current Drain 0.4 mA Typ
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Ω Typ
- Extremely Low Input Bias Current 1 pA Typ
- Ultra-Stable Low Input Offset Voltage
- Common-Mode Input Voltage Range Includes Ground
- Output Compatible with TTL, MOS, and CMOS

TLC374M . . . J DUAL-IN-LINE PACKAGE
TLC374C . . . D, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each of these devices features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships. The TLC374C is designed as a pin-compatible, functional replacement for the LM339, offering twice the speed while consuming typically one-half of the power.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374M is characterized for operation over the full military temperature range of −55 °C to 125 °C. The TLC374C is characterized for operation from 0 °C to 70 °C

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

TYPES TLC374M, TLC374C
QUADRUPLE LinCMOS™ DIFFERENTIAL COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC374M	TLC374C	UNIT
Supply voltage (see Note 1)		18	18	V
Differential input voltage (see Note 2)		±18	±18	V
Input voltage, V_I		18	18	V
Output voltage, V_O		18	18	V
Output current, I_O		20	20	mA
Duration of output short-circuit to ground (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, TLC374C chips are glass mounted and TLC374M chips are alloy mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC374M MIN	TLC374M TYP	TLC374M MAX	TLC374C MIN	TLC374C TYP	TLC374C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 5		25°C		2	10		2	10	mV
				Full range			12			12	
I_{IO}	Input offset current	See Note 5		25°C		1			1		pA
				Full range			10			0.3	nA
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			20			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} − 1.5			0 to V_{DD} − 1.5			V
				Full range	0 to V_{DD} − 2			0 to V_{DD} − 2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, R_L ≥ 15 kΩ to V_{CC}		25°C		200			200		v/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_{ID} = −1 V,	No load	25°C		0.4	1		0.4	1	mA

†All characteristics are measured with zero common-mode input voltage unless otherwise specified.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output up to 4 V or down to 400 mV with a pull-up resistor of 2.5 kΩ to V_{CC}. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance. Full range for T_A is −55°C to 125°C for TLC374M, 0°C to 70°C for TLC374C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

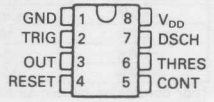
ADVANCE INFORMATION

TLC555M, TLC555I, TLC555C LinCMOS™ TIMERS

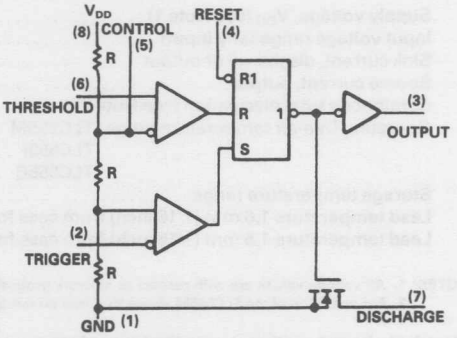
D2784 SEPTEMBER 1983—REVISED JUNE 1985

- **Very Low Power Consumption . . . 1mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V**
- **Functionally Interchangeable with the NE555; has same pin-out**

TLC555M . . . JG PACKAGE
TLC555I, TLC555C . . . D OR P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC555 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC555M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC555I is characterized for operation over the industrial temperature range of −40°C to 85°C. The TLC555C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

TLC555M, TLC555I, TLC555C
LinCMOS™ TIMERS

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation (see Note 2) . . . . . 460 mW
Operating free-air temperature range: TLC555M . . . . . −55°C to 125°C
TLC555I . . . . . −40°C to 85°C
TLC555C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation of the TLC555M above 95°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555I			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	0.95	1.33	1.65	0.95	1.33	1.65	V
		Full range	0.85		1.75	0.85		1.75	0.85		1.75	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	0.4	0.67	0.95	0.4	0.67	0.95	0.4	0.67	0.95	V
		Full range	0.3		1.05	0.3		1.05	0.3		1.05	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=1mA	25°C		0.03	0.2		0.03	0.2		0.03	0.2	V
		Full range			0.25			0.25			0.25	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=1mA	25°C		0.07	0.3		0.07	0.3		0.07	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH}=−300μA	25°C	1.5	1.9		1.5	1.9		1.5	1.9		V
		Full range	1.5			1.5			1.5			
Supply current		25°C		65	250		65	250		65	250	μA
		Full range			600			500			400	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I and 0°C to 70°C for TLC555C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555I			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=10mA	25°C		0.14	0.5		0.14	0.5		0.14	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=8mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5			0.5	
	I_{OL}=5mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4			0.4	
	I_{OL}=3.2mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply-current		25°C		170	350		170	350		170	350	µA
		Full range			700			600			500	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I and 0°C to 70°C for TLC555C.

TLC555M, TLC555I, TLC555C
LinCMOS™ TIMERS

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555I			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.77	1.7		0.77	1.7		0.77	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=100mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL}=50mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL}=10mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH}=−10mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH}=−5mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH}=−1mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			14.2			
Supply current		25°C		360	600		360	600		360	600	μA
		Full range			1000			900			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I and 0°C to 70°C for TLC555C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555I			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.72	1.5		0.72	1.5		0.72	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=3.2mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current		25°C		420	600		420	600		420	600	µA
		Full range			1000			900			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I and 0°C to 70°C for TLC555C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 µF. See Note 3		1%	3%	%/V
Supply voltage sensitivity of timing interval			0.1	0.5	
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF. See Note 3	1.2	2.1		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

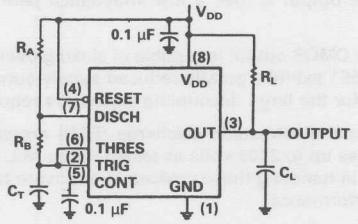


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

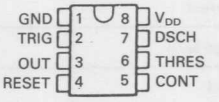
ADVANCE INFORMATION

TLC551C LinCMOS™ TIMER

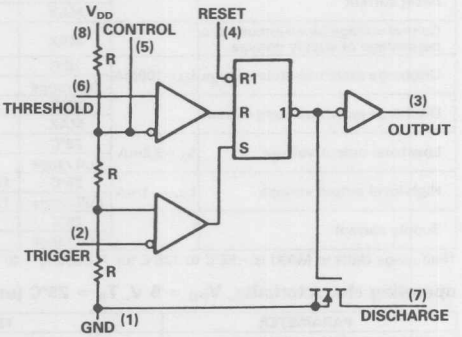
D2791 FEBRUARY 1984—REVISED JUNE 1985

- **Single-Supply Operation from 1 V to 18 V**
- **Very Low Power Consumption . . . 15 μW Typ at V_{DD} = 1V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Functionally Interchangeable with the NE555; has same pin-out**

TLC551C . . . D, JG OR P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC551 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC551 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC551C is characterized by operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

TLC551C
LinCMOS™ TIMER

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation . . . . . 460 mW
Operating free-air temperature range: TLC551C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.*

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		TLC551C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		0.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1.0	V
		Full range	0.3		1.0	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=100μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=100μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage		25°C	0.6	0.98		V
		Full range	0.6			
Supply current	I_{OH}=−10μA	25°C		15	100	μA
		Full range			150	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC551C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=1mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=1A	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH}=−300μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		65	250	μA
		Full range			400	

†Full range (MIN to MAX) is 0°C to 70°C.

TLC551C
LinCMOS™ TIMER

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC551C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=10mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=8mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL}=5mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL}=3.2mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		170	350	µA
		Full range			500	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC551C MIN	TLC551C TYP	TLC551C MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=100mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL}=50mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL}=10mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH}=−10mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH}=−5mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH}=−1mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		360	600	µA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

TLC551C
LinCMOS™ TIMER

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC551C MIN	TLC551C TYP	TLC551C MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=3.2mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		420	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF. See Note 3		1%	3%	
Supply voltage sensitivity of timing interval			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF. See Note 3	1.2	2.1		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

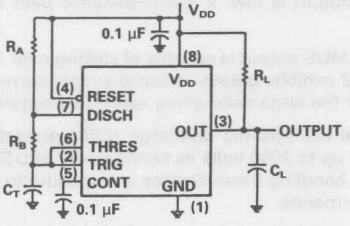


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

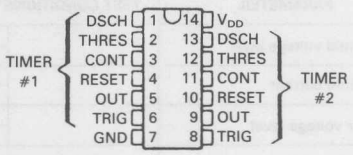
ADVANCE INFORMATION

TLC552C
DUAL LinCMOS™ TIMER

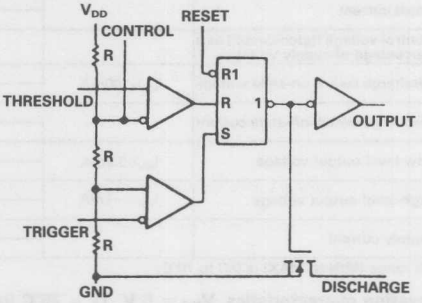
JUNE 1985

- **Single-Supply Operation from 1 V to 18 V**
- **Very Low Power Consumption . . . 30 μW Typ at V_{DD} = 1 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Functionally Interchangeable with the NE556; has same pin-out**

TLC552C . . . D, J OR N PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger, which can override Threshold.

description

The TLC552 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE556, the TLC552 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC552 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC552C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

TLC552C
DUAL LinCMOS™ TIMER

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation . . . . . 460 mW
Operating free-air temperature range: TLC552C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		TLC552C MIN	TLC552C TYP	TLC552C MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		0.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1.0	V
		Full range	0.3		1.0	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=100μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=100μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH}=−10μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		30	200	μA
		Full range			300	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC552C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=1mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=1mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH}=−300μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		130	500	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

TLC552C
DUAL LinCMOS™ TIMER

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC552C MIN	TLC552C TYP	TLC552C MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=10mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=8mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL}=5mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL}=3.2mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		340	700	µA
		Full range			1000	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC552C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=100mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL}=50mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL}=10mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH}=−10mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH}=−5mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH}=−1mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		720	1200	μA
		Full range			1600	

†Full range (MIN to MAX) is 0°C to 70°C.

TLC552C
DUAL LinCMOS™ TIMER

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC552C			UNIT
			MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL}=3.2mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		840	1200	μA
		Full range			1600	

†Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF. See Note 3		1%		%/V
Supply voltage sensitivity of timing interval			0.1		
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20		ns
Output pulse fall time			15		
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF. See Note 3		2.1		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

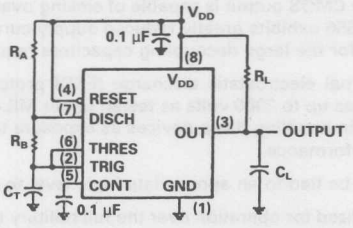


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

ADVANCE INFORMATION

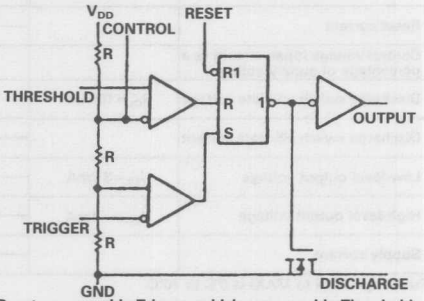
TLC556M, TLC556I, TLC556C DUAL LinCMOS™ TIMERS

D2796 FEBRUARY 1984—REVISED JUNE 1985

- **Very Low Power Consumption . . . 2mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V**
- **Functionally Interchangeable with the NE556, SA556 and SE556; has same pin-out**

TLC556M . . . J DUAL-IN-LINE PACKAGE
TLC556I, TLC556C . . . D OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

functional block diagram (each timer)



Reset can override Trigger, which can override Threshold.

description

The TLC556 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556M is characterized for operation over the full military temperature range of −55°C to 125°C.
The TLC556I is characterized for operation over the industrial temperature range of −40°C to 85°C.
The TLC556C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

TLC556M, TLC556I, TLC556C
DUAL LinCMOS™ TIMERS

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation (see Note 2) . . . . . 460 mW
Operating free-air temperature range: TLC556M . . . . . −55°C to 125°C
TLC556I . . . . . −40°C to 85°C
TLC556C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operating above 25°C free-air temperature, refer to Dissipation Derating Curves.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	0.95	1.33	1.65	0.95	1.33	1.65	0.95	1.33	1.65	V
		Full range	0.85		1.75	0.85		1.75	0.85		1.75	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	0.4	0.67	0.95	0.4	0.67	0.95	0.4	0.67	0.95	V
		Full range	0.3		1.05	0.3		1.05	0.3		1.05	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=1mA	25°C		0.03	0.2		0.03	0.2		0.03	0.2	V
		Full range			0.25			0.25			0.25	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=1mA	25°C		0.07	0.3		0.07	0.3		0.07	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH}=−300μA	25°C	1.5	1.9		1.5	1.9		1.5	1.9		V
		Full range	1.5			1.5			1.5			
Supply current		25°C		130	500		130	500		130	500	μA
		Full range			1200			1000			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I and 0°C to 70°C for TLC556C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=10mA	25°C		0.14	0.5		0.14	0.5		0.14	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=8mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5			0.5	
	I_{OL}=5mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4			0.4	
	I_{OL}=3.2mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current		25°C		340	700		340	700		340	700	µA
		Full range			1400			1200			1000	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I and 0°C to 70°C for TLC556C.

TLC556M, TLC556I, TLC556C
DUAL LinCMOS™ TIMERS

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.77	1.7		0.77	1.7		0.77	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=100mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL}=50mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL}=10mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH}=−10mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH}=−5mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH}=−1mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			14.2			
Supply current		25°C		720	1200		720	1200		720	1200	µA
		Full range			2000			1800			1600	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I and 0°C to 70°C for TLC556C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL}=100mA	25°C		0.72	1.5		0.72	1.5		0.72	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL}=3.2mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH}=−1mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current		25°C		840	1200		840	1200		840	1200	μA
		Full range			2000			1800			1600	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I and 0°C to 70°C for TLC556C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF. See Note 3		1%		%/V
Supply voltage sensitivity of timing interval			0.1		
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20		ns
Output pulse fall time			15		
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF. See Note 3		2.1		MHz

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

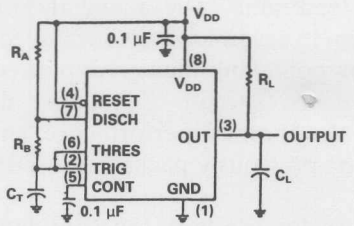


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

Packaging Information

PLASTIC SMALL OUTLINE (SO) PACKAGE

Surface-mounted components

The SOIC package is the preferred surface mount component for low pin-count integrated circuits because it can be made smaller than the chip carrier which has a practical lower limit of 18 pins.

Because the SOIC package has dual-in-line leads it can be easier to layout high density PCBs than is the case with chip carriers which have leads around the full perimeter. This is acceptable for a low lead-count SOIC package because it is smaller than the equivalent chip carrier.

The leads are on the standard 1.27 mm centres and they are formed out in an inverted "Gull Wing" fashion so that the lead tips lay flat on the surface of the PCB.

The SOIC devices are constructed using the same chips and similar assembly techniques and therefore meet the same data sheet electrical parameters as the equivalent Dual-In-Line device.

Thermal characteristics of SO packages

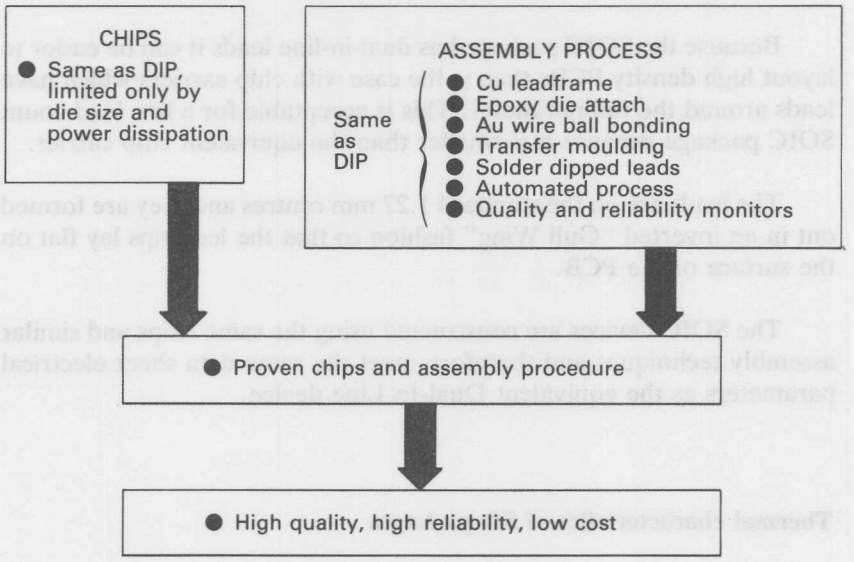
The thermal dissipation capability of the SO package is similar to that of the equivalent Dual-In-Line plastic device constructed using the standard Alloy 42 leadframe. The actual thermal impedance of any device will depend upon several factors such as the silicon chip size and type of moulding compound but the curves plotted alongside are typical for comparable products. The use of a copper alloy leadframe for the SO has optimised the thermal performance and ensures continuing reliability of products previously packaged in DIP packages.

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

Junction-to-ambient thermal resistance $R_{\theta JA}$ measurement specimens are mounted in a socket which is mounted to a printed circuit card in still air.

Contact TI Customer Response Centre for further information on Surface Mounted Packaging and techniques.

SO package assembly procedure

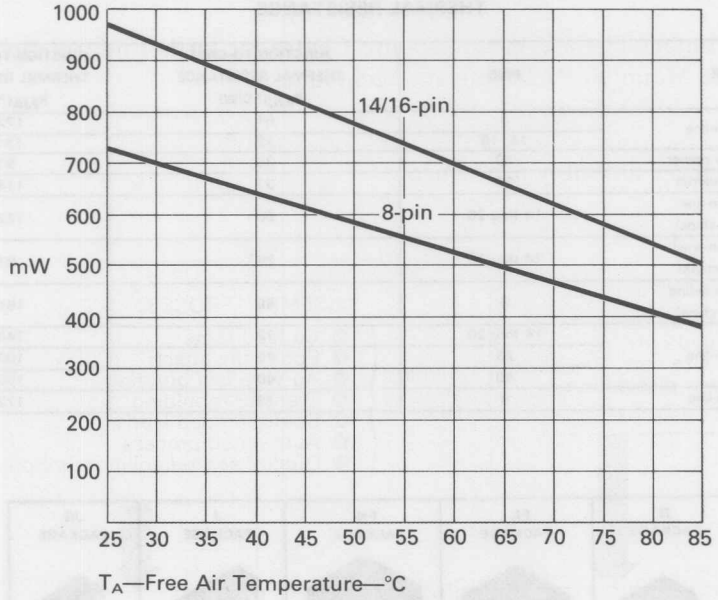


Thermal information SO package

Package	Pins	Junction to case thermal resistance $R_{\theta JC}$ (°C/W)	Junction to ambient thermal resistance $R_{\theta JA}$ (°C/W)	Power rating	Derating factor	Above T_A
D plastic (SO)	8	51	172	725 mW	5.8 mW/°C	25°C
	14, 16	33	130	950 mW	7.7 mW/°C	25°C
	20	15*	75*			

*Preliminary data.

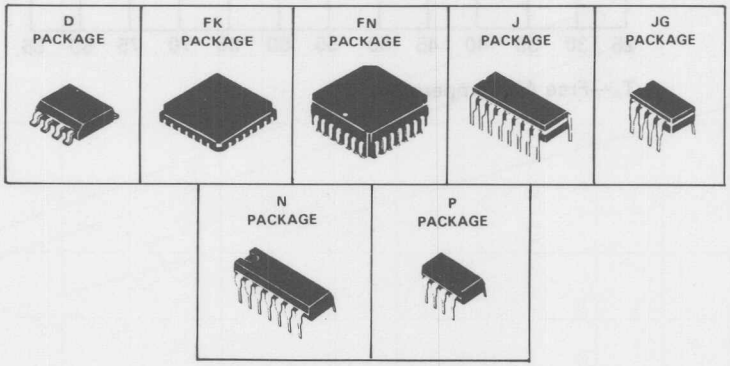
Dissipation derating curve



THERMAL INFORMATION

THERMAL RESISTANCE

PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$(°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$(°C/W)
D plastic dual-in-line	8	51	172
	14, 16	33	131
FK ceramic chip carrier	20	35	91
FN plastic chip carrier	20	37	114
J ceramic dual-in-line (glass-mounted chips)	14 thru 20	60	122
J ceramic dual-in-line† (alloy-mounted chips)	14 thru 20	29†	91†
JG ceramic dual-in-line (glass-mounted chips)	8	58	151
N plastic dual-in-line	14 thru 20	72	143
	28	45	100
	40	40	100
P plastic dual-in-line	8	79	172

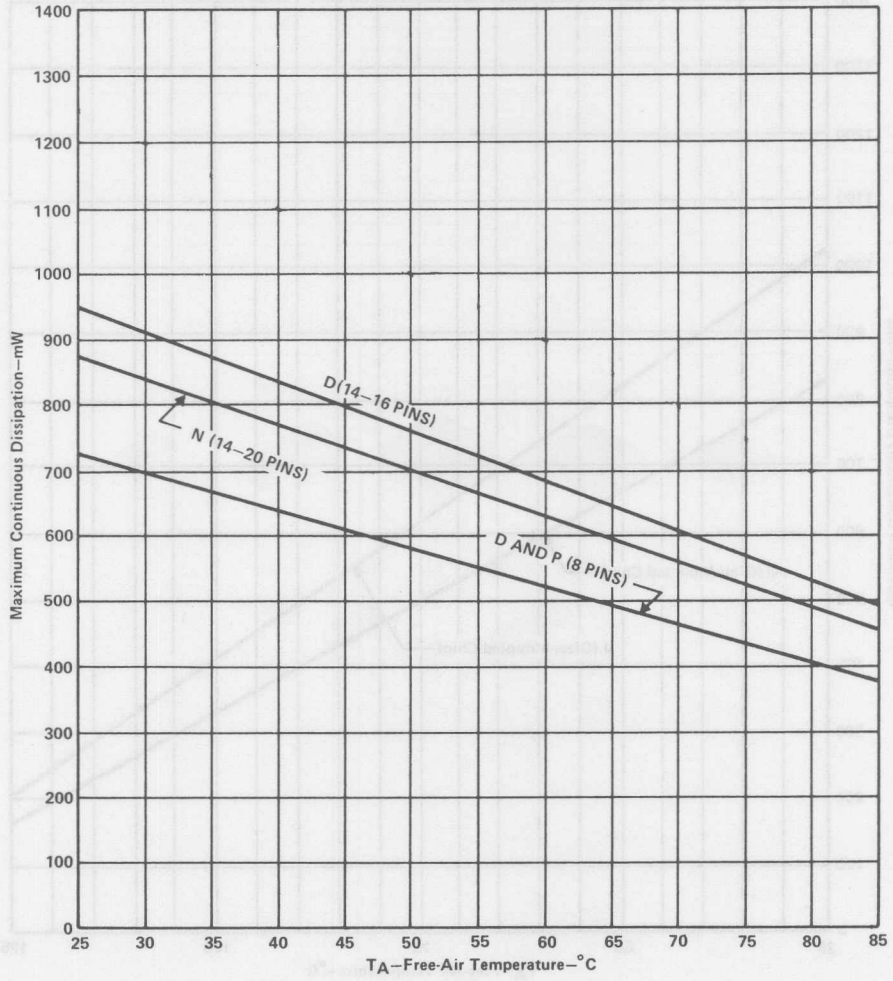


THERMAL INFORMATION

PLASTIC PACKAGES (CONTINUED)

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE

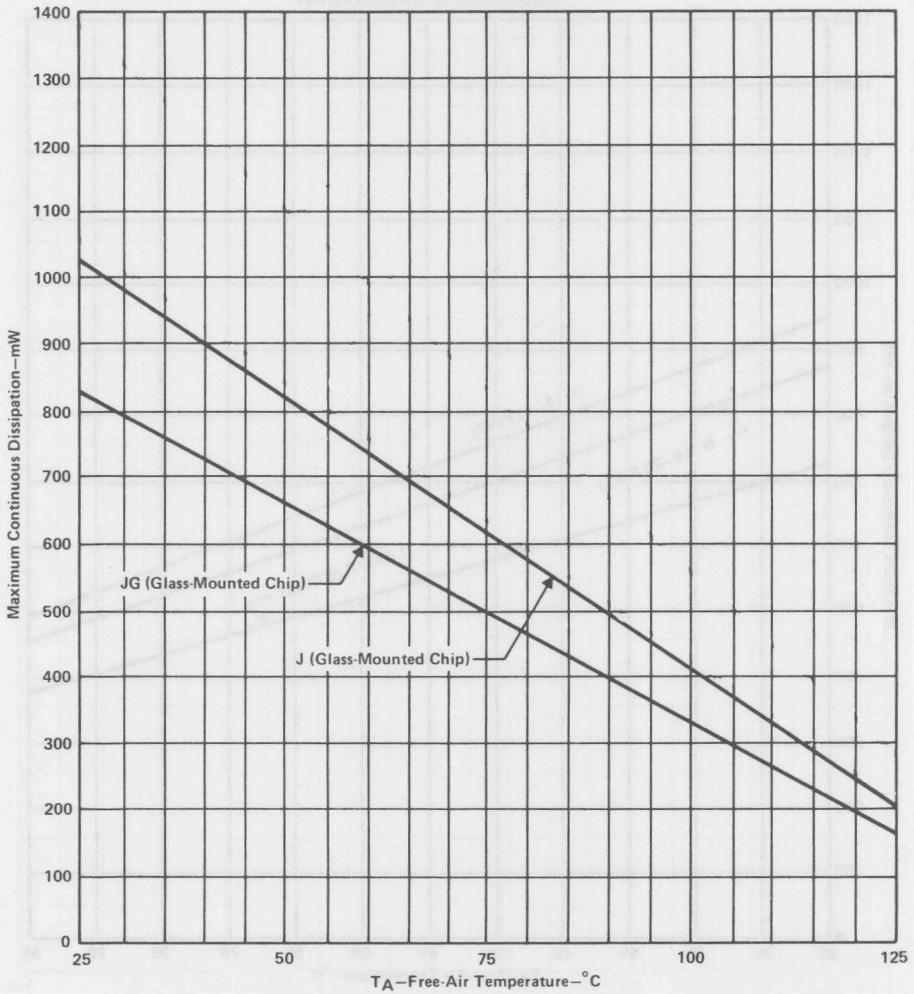


THERMAL INFORMATION

CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE

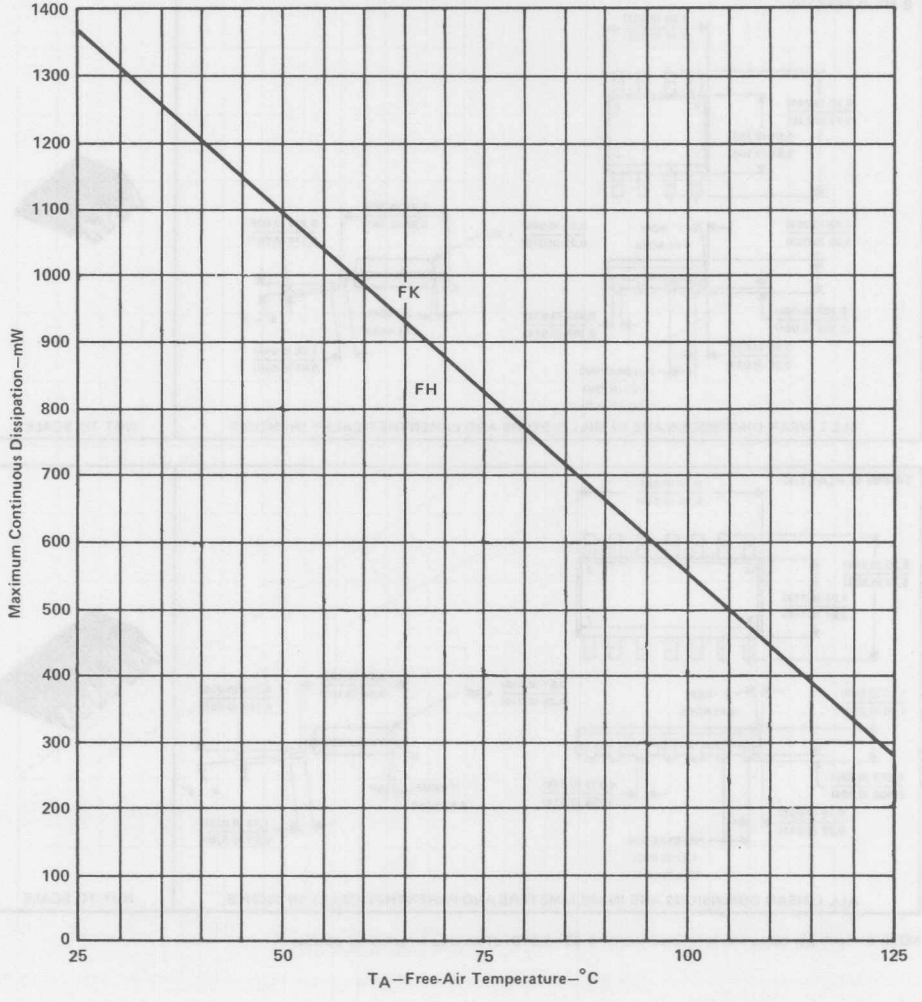


†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883B" have alloy-mounted chips.

FLAT PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE

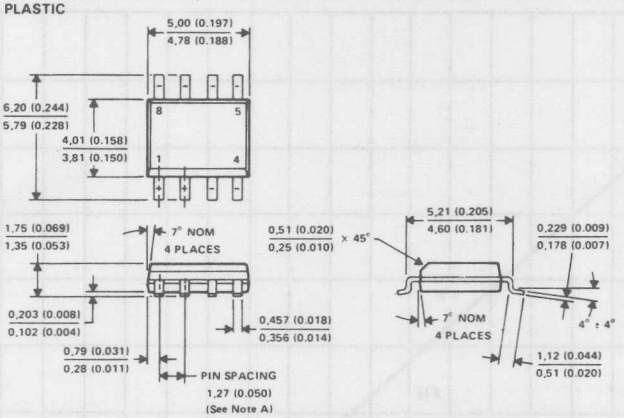


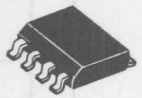
MECHANICAL DATA

D plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

8-PIN D PLASTIC

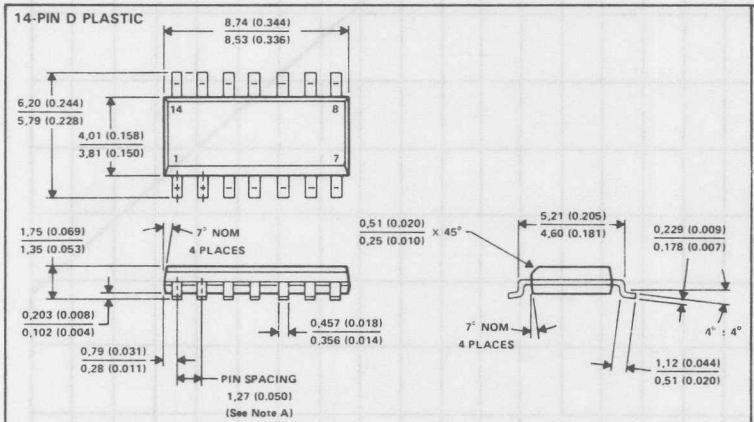


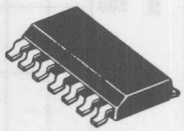


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

14-PIN D PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

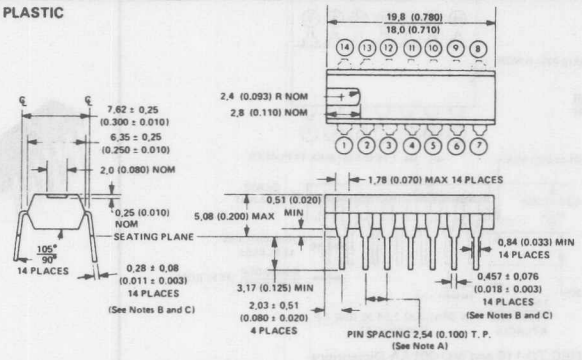
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

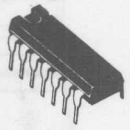
MECHANICAL DATA

N plastic dual-in-line package

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC



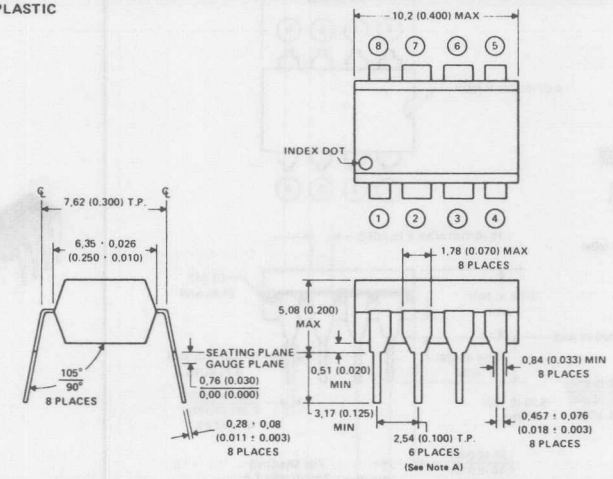


Falls Within JEDEC TO 116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

8-PIN P PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

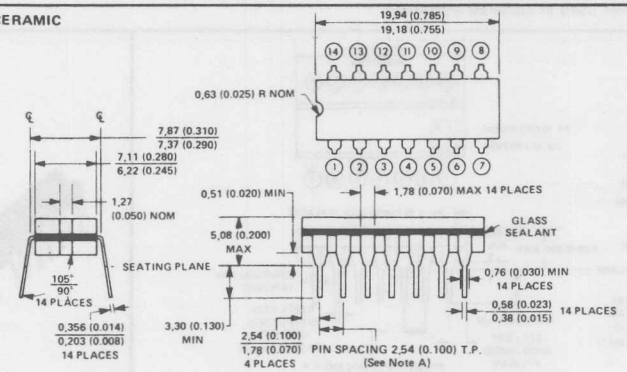
NOTE A: Each pin centerline is within 0,13 (0.005) radius of true position at the gauge plane with maximum material condition and unit installed.

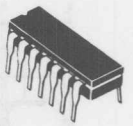
MECHANICAL DATA

J ceramic dual-in-line packages

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

14-PIN J CERAMIC

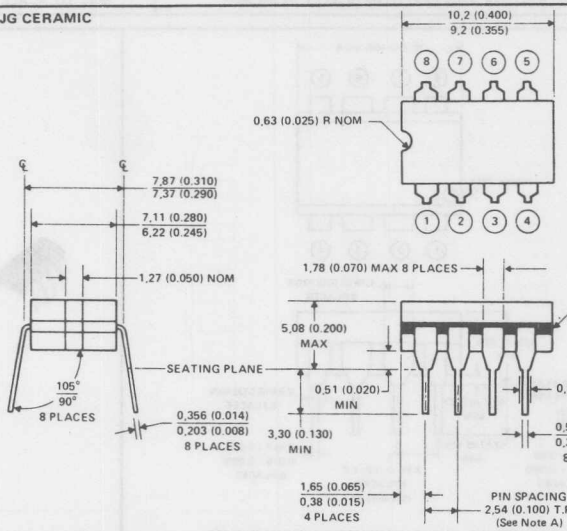




Falls Within JEDEC TO-116 and MO-001AA Dimensions
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

8-PIN JG CERAMIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

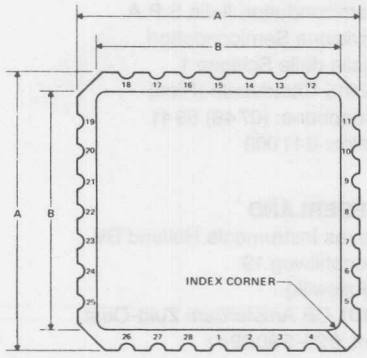
FH and FK ceramic chip carrier packages

Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FH package is an all-ceramic package with a glass seal. The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FH and FK package terminal assignments conform to JEDEC Standards 1 and 2.

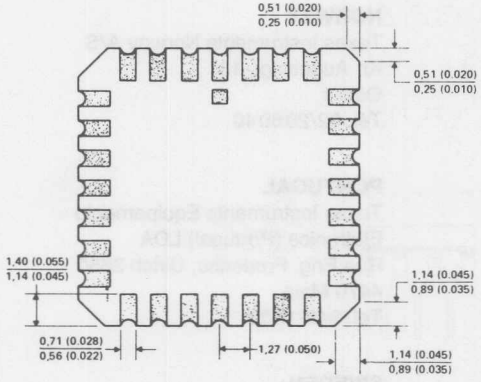
FH AND FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)

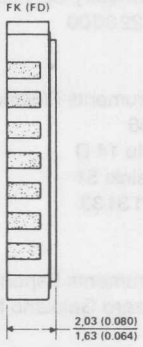


CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

TEXAS INSTRUMENTS

AUSTRIA
Texas Instruments Ges.m.b.H.
Industriestraße B/16
A-2345 Brunn am Gebirge
Tel. 02236/84621-0

BELGIUM
Texas Instruments Belgium N.V.
Mercure Centre
Raketstraat 100, Rue de la Fusee
1130 Brussels
Tel. 02/7208000

DENMARK
Texas Instruments A/S
Marielundvej 46 E
2730 Herlev
Tel. 02/917400

ENGLAND
Texas Instruments Ltd.
Manton Lane
Bedford, MK 41 7 PA
Tel. 0234/67466
Technical Enquiry Service:
Tel. 0234/223000

FINLAND
Texas Instruments Finland OY
P.O. Box 56
Elimaenkatu 14 D
00511 Helsinki 51
Tel. 90/70131 33

ESPANA
Texas Instruments Espana S.A.
C/Jose Lazaro Galdiano No. 6
16 Madrid
Telephone: (34) 1-4581458

FRANCE
Texas Instruments France
Boite Postale 5
06270 Villeneuve-Loubet
Tel. 093/200101

GERMANY
Texas Instruments Deutschland GmbH
Haggertystraße 1
8050 Freising
Tel. 08161/80-0

ITALIA
Texas Instruments
Semiconduttori Italia S.P.A.
Divisione Semiconduttori
Vialle delle Scienze 1
02015 Cittaducale (Rieti)
Telephone: (0746) 6941
Telex: 611003

NEDERLAND
Texas Instruments Holland BV.
Hogehilweg 19
(Bullewijk)
1101 CB Amsterdam Zuid-Oost
Tel. 020-5602911

NORWAY
Texas Instruments Norway A/S
Kr. Augustsgt. 13
Oslo 1
Tel. 02/206040

PORTUGAL
Texas Instruments Equipamento
Eletronico (Portugal) LDA
Rua Eng. Frederico, Ulrich 2650
4470 Maia
Tel. 948-1003

SWEDEN
Texas Instruments International
– Trade Corporation
(Sverigefilialen)
Box 39103
10054 Stockholm
Tel. 08/235480